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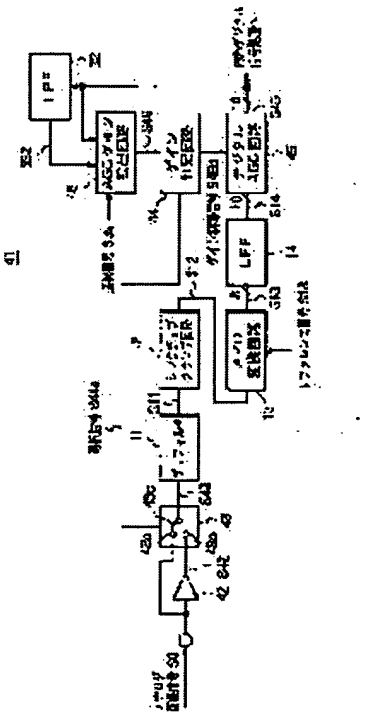
(54) PICTURE SIGNAL PROCESSING CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To enable a circuit structure on a small-scale to execute a gain control with high accuracy by detecting a gain of an outputting signal by way of a level adjustment means, after converting an inputted analog picture to a digital picture signal and controlling the level adjustment means of a level of analog picture signal and a level of digital picture signal on the basis of a detected gain.
SOLUTION: An analog picture signal S42 selected by a selector 43 or an analog picture signal S 42 amplified by an amplification circuit 42 is converted into a digital picture signal at an A/D converting circuit 13, gain controlled at a digital AGC circuit 45 and outputted as a digital picture signal S45. A gain discrimination circuit 44 controls the selector 43 and the digital AGC circuit 45, on the basis of a gain detection signal S 46. Thus, a gain control can be executed with high accuracy by executing a rough gain control at the selector 43 and a fine gain control at the digital AGC circuit 45, and a circuit can be made relatively small.



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CLAIMS

[Claim(s)]
[Claim 1]A picture signal processing circuit comprising:
The singular number which amplifies an inputted analog picture signal by a predetermined gain, or two or more amplifying means.
A selecting means which chooses an analog picture signal of 1 from two or more analog picture signals based on a selection signal for analog picture signal selection among said inputted analog picture signal and said amplified analog picture signal.
An analog-to-digital conversion means to change said selected analog picture signal into digital image data.
A level adjustment means to adjust a level of said digital image signal by a gain according to a control signal, A gain detection means to detect a gain of a digital image signal with which said level was adjusted, and a gain judging means which generates a selection signal and said control signal for said analog picture signal selection based on said detected gain.

[Claim 2]Said gain judging means A gain of said amplifying means, and an input dynamic range of said analog-to-digital conversion means, Based on said gain detection result, inside of two or more of said analog picture signals, The picture signal processing circuit according to claim 1 which generates a selection signal for analog picture signal selection which shows that an analog picture signal with a gain nearest to an input dynamic range of said analog-to-digital conversion means is chosen.
[Claim 3]The picture signal processing circuit according to claim 1 where said selecting means chooses an analog picture signal of one among said inputted analog picture signal and said amplified analog picture signal.
[Claim 4]From a digital image signal from said level adjustment means, have further a synchronized signal extraction means to extract a synchronized signal, and said gain detection means, The picture signal processing circuit according to claim 1 which detects a gain of one signal based on a selection signal for gain detecting-signal selection among a digital image signal from said level adjustment means, and a synchronized signal from said synchronized signal extraction means.
[Claim 5]The picture signal processing circuit according to claim 4 in which said synchronized signal extraction means is a low pass filter.
[Claim 6]The picture signal processing circuit according to claim 4 which detects a gain of said digital-image-data signal after said gain detection means detects a gain of said synchronized signal.
[Claim 7]When selection of an analog picture signal by a selection signal for analog picture signal selection switches within predetermined time in more than prescribed frequency, said gain judging means, The picture signal processing circuit according to claim 1 which changes a gain judging level of a gain detection result used when generating a selection signal for analog picture signal selection.

[Claim 8]When selection of an analog picture signal by a selection signal for analog picture signal

selection switches within predetermined time in more than prescribed frequency, said gain judging means, The picture signal processing circuit according to claim 1 which lowers a gain judging level of a gain detection result used when generating a selection signal for analog picture signal selection.
[Claim 9]The picture signal processing circuit according to claim 1 which amplifies by a gain which fixed said amplifying means.
[Claim 10]The picture signal processing circuit according to claim 1 whose gain of said amplifying means is variable.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to a picture signal processing circuit.
[0002]
[Description of the Prior Art]For example, NTSC (National Television Committee) which received A method and PAL (Phase Alternation by Line) To the decoder of the receiving set which carries out digital processing, the analog picture signal of a method usually, A (Analog)/D (Digital) which changes the received analog picture signal into digital image data The conversion circuit is built in. If the electric wave induced by the antenna has strength for example, the received analog picture signal will be changed similarly and the contrast of a screen, etc. will change. In order to use as a predetermined level the level of the analog picture signal received to the decoder of the receiving set in order to avoid this, the AGC (Automatic Gain Control) circuit which controls a gain is built in.
[0003]The picture signal processing circuit hereafter provided with the A/D conversion circuit and AGC circuit which were built in the decoder of the conventional receiving set is explained. Drawing 6 is the lineblock diagram of the picture signal processing circuit 1 which performs gain detection with an analog form and performs gain control with an analog form built in the decoder of the conventional receiving set. In the picture signal processing circuit 1, the analog picture signals S0, such as a luminance signal, a composite signal, or a chrominance signal, are inputted, and the gain control amplifier 10 performs gain control for this analog picture signal S0 based on the gain detecting signal S16 from the AGC gain detector circuit 16. The analog picture signal S10 from the gain control amplifier 10 is outputted to the low pass filter (LPF) 15, the AGC gain detector circuit 16, and the pre-filter 11.
[0004]Horizontal high-frequency components, such as a subcarrier, are removed by the low pass filter 15, and, as for the analog picture signal S10, the analog picture signal S15 restricted to 1 MHz is outputted for a zone to the AGC gain detector circuit 16. the synchronized signal with which the analog picture signal S15 is included in the analog picture signal S0 here -- abbreviated -- it is the same. In the AGC gain detector circuit 16, gain detection is selectively performed based on the selection signal S19 about the analog picture signal S15 from the low pass filter 15, and the analog picture signal S10 from the gain conte row amplifier 10, The gain control signal S16 according to the gain detection concerned is outputted to the gain control amplifier 10.
[0005]Specifically in the AGC gain detector circuit 16. When the analog picture signal S15 is chosen, gain detection is performed about the synchronized signal contained in the analog picture signal S0, and feedback gain control is performed about the synchronized signal concerned in the gain control amplifier 10. For example, feedback gain control is performed so that the gain of a synchronized signal may become with 401IRE in the case of NTSC system and may become with 431IRE in the case of a PAL system.
[0006]On the other hand, in the AGC gain detector circuit 16, when the analog picture signal S10 is

chosen, in the gain control amplifier 10 and the AGC gain detector circuit 16, gain control is performed about the signal of all the zones included in the analog picture signal S0. That is, feedback gain control is performed so that the peak level of the analog picture signal S0 may be settled in a predetermined range. For example, as the input dynamic ranges in the A/D conversion circuit 13 are 1.500 ****-p and it is shown in drawing 7 and drawing 8, When the peak level of the 100% of analog image color bar signal S0 is as low as 1.243V and 0.621V, the gain control amplifier 10 performs gain control so that a peak level may generate the analog picture signal S10 used as 1.434V. As shown in drawing 9, when the peak level of the 100% of analog image color bar signal S0 is as high as 1.912V, the gain control amplifier 10 performs gain control so that a peak level may generate the analog picture signal S10 used as 1.434V.

[0007]The analog picture signal S10 is band-limited in the pre-filter 11 so that aliasing may not arise at the time of the A/D conversion in the latter A/D conversion circuit 13. This band-limited analog picture signal S11 is adjusted to bottom product potential [in / in that bottom product potential / the A/D conversion circuit 13] in the sink chip clamp circuit 12. In [in the A/D conversion circuit 13, the A/D conversion of the analog picture signal S12 is carried out by the quantization step according to the reference signal S18, and] LPF14 this 8-bit digital image signal S13, A horizontal high-frequency component is removed, for example, it becomes the digital image signal S14 which is 10 bits.

[0008]Drawing 10 is the lineblock diagram of the picture signal processing circuit 21 which performs gain detection with a digital system and performs gain control with an analog form built in the decoder of the conventional receiving set. In the picture signal processing circuit 21, the digital image signal S14 from LPF14 is outputted to LPF22 and the AGC gain detector circuit 26. In LPF22, horizontal high-frequency components, such as a subcarrier, are removed, a zone is restricted to 1 MHz, and the digital image signal S14 turns into the digital image signal S22. The digital image signal S22 is equivalent to what carried out the A/D conversion of the synchronized signal contained in the analog picture signal S0. In the AGC gain detector circuit 26, gain detection is selectively performed based on the selection signal S29 about the digital image signal S14 from the digital image signals S22 and LPF14 from the low pass filter 22, The digital gain control signal S26 according to the gain detection concerned is outputted to the D/A conversion circuit 23. D/A conversion of the gain control signal S26 is carried out to the gain control signal S23 of an analog in the D/A conversion circuit 23. Based on the gain control signal S23, feedback gain control of the analog picture signal S0 is carried out in the gain control amplifier 20.

[0009]Drawing 11 is the lineblock diagram of the picture signal processing circuit 31 which performs gain detection with a digital system and performs gain control with a digital system built in the decoder of the conventional receiving set. The analog picture signal S0 is processed in pre-filter 11, sink chip clamp circuit 12, A/D conversion circuit 13, and LPF14, and is inputted into digital AGC30 as the digital image signal S14. Based on the gain control signal S33 of digital format, feedback gain control is carried out and the digital image signal S14 is outputted as the digital image signal S30. The digital image signal S30 is outputted to LPF32 and the AGC gain detector circuit 33. About the digital image signal S32 and the digital image signal S30 corresponding to a synchronized signal, based on the selection signal S39, the AGC gain detector circuit 33 performs gain detection selectively, and outputs the gain control signal S33 according to the detection result concerned to digital AGC30.

[0010]

[Problem(s) to be Solved by the Invention]However, in the picture signal processing circuit 1 shown in drawing 6 mentioned above. Since feedback control of the gain control amplifier 10 is carried out by the analog form with the gain control signal S16 from the AGC gain detector circuit 16, it is difficult to realize linear gain control, and development time will delay. It is not easy to design the circuit in which the transistor of CMOS which constitutes the gain control amplifier 10 specifically has the desired characteristic.

[0011]In the picture signal processing circuit 21 shown in drawing 10 mentioned above, since the gain control signal S26 is generated by digital format in the AGC gain detector circuit 26, can perform gain control with high precision, but. Since the D/A conversion circuit 23 is generally formed, there is a problem that a circuit will large-scale-ize.
[0012]In the picture signal processing circuit 31 shown in drawing 11 mentioned above. Since gain control is performed by digital format after an A/D conversion, when the amplitude of the analog picture signal S0 is small, The A/D conversion fully using the input dynamic range of the A/D conversion circuit 13 will not be able to be performed, but quantization will become rude, and image quality deterioration will be an intense dirty picture under the influence of a quantization noise.
[0013]This invention is made in view of the conventional technology mentioned above, is small-scale circuitry, and can perform gain control with high precision, and an object of this invention is to provide comparatively simply the picture signal processing circuit which can be developed.
[0014]
[Means for Solving the Problem]In order to solve a problem of conventional technology mentioned above and to attain the purpose mentioned above, a picture signal processing circuit of this invention is provided with the following.
The singular number which amplifies an inputted analog picture signal by a predetermined gain, or two or more amplifying means.
A selecting means which chooses an analog picture signal of 1 from two or more analog picture signals based on a selection signal for analog picture signal selection among said inputted analog picture signal and said amplified analog picture signal.
An analog-to-digital conversion means to change said selected analog picture signal into digital image data.
A level adjustment means to adjust a level of said digital image signal by a gain according to a control signal, A gain detection means to detect a gain of said digital image signal by which level adjustment was carried out, and a gain judging means which generates a selection signal and said control signal for said analog picture signal selection based on said detected gain.

[0015]A picture signal processing circuit of this invention determines then an analog picture signal chosen in a selecting means in a gain judging means based on a gain detection result. Therefore, based on a gain detection result, an amplification factor of an inputted analog picture signal can be determined, and an inputted analog picture signal can be amplified so that an input dynamic range of processing may be efficiently used at the time of conversion in an analog-to-digital conversion means. In a gain judging means, since a level adjustment means of a digital system is controlled based on a gain detected by a gain detection means, a digital system can perform highly precise level adjustment (AGC), i.e., automatic gain control.
[0016]
[Embodiment of the Invention]Hereafter, the picture signal processing circuit concerning the embodiment of this invention is explained. In the conventional picture signal processing circuit, when carrying out the A/D conversion of the analog picture signals, such as NTSC system or a PAL system, The both sides of an analog form and a digital system perform double feedback control in the picture signal processing circuit of this embodiment to having performed gain control by either one of the analog form or the digital system.
[0017]1st embodiment drawing 1 is a lineblock diagram of the picture signal processing circuit 41 of this embodiment. As shown in drawing 1, the picture signal processing circuit 41 is provided with the amplifying circuit 42, the selector 43, the pre-filter 11, the sink chip clamp circuit 12, the A/D conversion circuit 13, LPF14, the digital AGC circuit 45, LPF32, the AGC gain detector circuit 46, and the gain decision circuit 44. Here, the pre-filter 11, the sink chip clamp circuit 12, and the A/D conversion circuit 13 are the same as the component of the identical codes of the picture signal processing circuit 1 shown in drawing 5. LPF32 is the same as the component of the identical codes

of the picture signal processing circuit 31 shown in drawing 10. The picture signal processing circuit 41 is built in the decoder of the receiving set which carries out digital processing of the analog picture signal of the NTSC system and the PAL system which were received, for example.

[0018]The amplifying circuit 42 inputs the analog picture signals S0, such as a luminance signal, a composite signal, or a chrominance signal, amplifies this analog picture signal S0 of only 6 dB, and outputs the amplified analog picture signal S42 to the input terminal 43b of the selector 43. Based on the selection signal S44a from the gain decision circuit 44 (for example, 1 bit), the selector 43 switches the switch 43c between the input terminal S43a and S43b, and outputs selectively the analog picture signal S0 or S42 to the pre-filter 11 as the analog picture signal S43.

[0019]The pre-filter 11 performs filtering to the analog picture signal S43, and restricts frequency to a predetermined zone so that aliasing may not occur at the time of an A/D conversion. The sink chip clamp circuit 12 adjusts the bottom product potential of the analog picture signal S11 from the pre-filter 11 to the bottom product potential in the A/D conversion in the A/D conversion circuit 13, and outputs this adjusted analog picture signal S12 to the A/D conversion circuit 13.

[0020]The A/D conversion circuit 13 carries out the A/D conversion of the analog picture signal S12 by the quantization step according to the reference signal S18, and outputs the 8-bit digital image signal S13 to LPF14. To the digital image signal S13, LPF14 performs filtering, and removes a horizontal broader-based ingredient, for example, outputs the 10-bit digital image signal S14 to the digital AGC circuit 45.

[0021]Based on the gain control signal S44b from the gain decision circuit 44, the digital AGC circuit 45 performs feedback gain control of a digital system to the digital image signal S14, and outputs the digital image signal S45 concerned by which gain control was carried out. LPF32 removes horizontal high-frequency components, such as a subcarrier, to the digital image signal S45 from the digital AGC circuit 45, and a zone outputs the digital image signal S32 restricted to about 1 MHz to the AGC gain detector circuit 46. The digital image signal S32 is a digital signal corresponding to the synchronized signal contained in the analog picture signal S0.

[0022]According to the selection signal S39, the AGC gain detector circuit 46 about the digital image signal S32 from LPF32, and the digital image signal S45 from the digital AGC circuit 45. Selectively, a digital system performs gain detection and the gain detecting signal S46 according to the detection result concerned is outputted to the gain decision circuit 44. When the selection signal S39 is pointing to detection of the sink level, the AGC gain detector circuit 46 performs gain detection of the digital image signal S32, and, specifically, detects the sink level of the synchronized signal contained in the digital image signal S45. On the other hand, when the selection signal S39 is pointing to detection of the Max level, the AGC gain detector circuit 46 performs gain detection of the digital image signal S45, and detects the peak level of the digital image signal S45. For example, a peak level can be adjusted after adjusting the sink level of the digital image signal S45 in the digital AGC circuit 45 by making it direct detection of the Max level after the selection signal S39 points to detection of a sink level.

[0023]The gain decision circuit 44 receives the amplitude of the analog picture signal S12 based on the gain detecting signal S46, When it judges whether the input dynamic range of the A/D conversion circuit 13 is generous and it is judged that it is generous, the selection signal S44a which shows that it switches to the input terminal 43b is outputted to the selector 43. Here, the input dynamic ranges of the A/D conversion circuit 13 are 0-1.500V, for example. On the other hand, the gain decision circuit 44 outputs the selection signal S44a with which ****** shows that it switches to the input terminal 43a at a case if a margin does not have an input dynamic range of the A/D conversion circuit 13 to the amplitude of the analog picture signal S12 at the selector 43. Based on the gain detecting signal S46, when the peak level of the analog picture signal S12 is below half of the input dynamic range of the A/D conversion circuit 13, it specifically judges that it is generous, and in being larger than a half, it judges that it is hard-pressed.

[0024]The gain decision circuit 44 generates the gain control signal S44b for carrying out feedback

gain control of the digital image signal S45 in the digital AGC circuit 45 at a predetermined level based on the gain detecting signal S46, and outputs this to the digital AGC circuit 45.
[0025]Hereafter, operation of the picture signal processing circuit 41 shown in drawing 1 is explained. First, the peak of the amplitude of the analog picture signal S0 explains the case where it is below half (0.750V) of the input dynamic range (1.500V) of the A/D conversion circuit 13. In this case, in the gain decision circuit 44 based on the gain detecting signal S46, The selection signal S44a which shows that a switch is switched to the input terminal 43b is outputted to the selector 43, and the analog picture signal S42 which amplified the analog picture signal S0 of only 6 dB is outputted to the pre-filter 11 as the analog picture signal S43. That is, the analog picture signal S43 which doubled the amplitude of the analog picture signal S0 is outputted to the pre-filter 11.
[0026]It is band-limited in the pre-filter 11, bottom product potential is adjusted in the sink chip clamp circuit 12, and the A/D conversion of the analog picture signal S43 is carried out in the A/D conversion circuit 13, and it is outputted to LPF14 as the 8-bit digital image signal S13. In LPF14, a horizontal high-frequency component is removed and the digital image signal S13 turns into the digital image signal S14 which is 10 bits. Based on the selection signal S39 which shows that the digital image signal S14 chooses the analog picture signal S32, By first, the feedback control of the digital system by the digital AGC circuit 45, LPF32, the AGC gain detector circuit 46, and the gain decision circuit 44. For example, gain control of the sink level is carried out so that it may be set to 401IRE in the case of NTSC system, and it may be set to 431IRE in the case of a PAL system. Next, the selection signal S39 switches so that choosing the analog picture signal S45 may be shown, and the digital image signal S14, Gain control is carried out so that a peak level may fill a regular range by the feedback control of the digital system by the digital AGC circuit 45, the AGC gain detector circuit 46, and the gain decision circuit 44.
[0027]Next, the peak of the amplitude of the analog picture signal S0 explains the case where it is larger than the half (0.750V) of the input dynamic range (1.500V) of the A/D conversion circuit 13. In this case, based on the gain detecting signal S46, in the gain decision circuit 44, the selection signal S44a which shows that a switch is switched to the input terminal 43a is outputted to the selector 43, and the analog picture signal S0 is outputted to the pre-filter 11 as the analog picture signal S43.
[0028]It is band-limited in the pre-filter 11, bottom product potential is adjusted in the sink chip clamp circuit 12, and the A/D conversion of the analog picture signal S43 is carried out in the A/D conversion circuit 13, and it is outputted to LPF14 as the 8-bit digital image signal S13. In LPF14, a horizontal high-frequency component is removed and the digital image signal S13 turns into the digital image signal S14 which is 10 bits. Subsequent processing is the same as the case where the peak of the amplitude of the analog picture signal S0 mentioned above is below half (0.750V) of an input dynamic range (1.500V).
[0029]As explained above, since feedback control of the gain of the digital image signal S14 is carried out with a digital system, highly precise gain control can be performed in the picture signal processing circuit 41 by the digital AGC circuit 45, the AGC gain detector circuit 46, and the gain decision circuit 44. That is, according to the picture signal processing circuit 41, the quality digital image signal acquired by carrying out the A/D conversion of the analog picture signal S0 of NTSC system or a PAL system can be outputted to a latter digital signal processing circuit. In the picture signal processing circuit 41, below half of the input dynamic range of the A/D conversion circuit 13 outputs the analog picture signal S12 which amplified the amplitude of the analog picture signal S0 twice to the A/D conversion circuit 13, when the amplitude of the peak level of the analog picture signal S0 is very low. Therefore, it can avoid effectively that quantization precision becomes rude to the analog picture signal S0 with a low peak level of amplitude like the picture signal processing circuit 31 shown in drawing 10 mentioned above, and the influence of a quantization noise can be reduced.
[0030]In order that giving the desired characteristic like the picture signal processing circuit 1

shown in drawing 5 only with outputting the several bits selection signal S44a to the selector 43 may not perform gain control of a difficult analog form according to the picture signal processing circuit 41, a circuit design is easy and a development cycle is also short.

[0031]Like the picture signal processing circuit 21 shown in drawing 9, since a D/A conversion circuit is not used, small-scale circuitry is realizable in the picture signal processing circuit 41.

[0032]Namely, according to the picture signal processing circuit 41, the analog picture signal S0 is received, The gain decision circuit 44, the amplifying circuit 42, and the selector 43 perform rude gain control by an analog form, After an A/D conversion, by performing gain control finely with a digital system by the digital AGC circuit 45, the AGC gain detector circuit 46, and the gain decision circuit 44. Highly precise gain control with little influence of a quantization noise can be performed, a circuit design is easy, a development cycle is short, and, moreover, a circuit can be made comparatively small-scale.

[0033]2nd embodiment drawing 2 is a lineblock diagram of the picture signal processing circuit 51 of this embodiment. As shown in drawing 2, the picture signal processing circuit 51, It has the amplifying circuits 56, 57, 58, and 59, the selector 53, the pre-filter 11, the sink chip clamp circuit 12, the A/D conversion circuit 13, the column decoder 14, the digital AGC circuit 45, LPF32, the AGC gain detector circuit 46, and the gain decision circuit 54. Here, the pre-filter 11 shown in drawing 2, the sink chip clamp circuit 12, the A/D conversion circuit 13, the column decoder 14, the digital AGC circuit 45, LPF32, and the AGC gain detector circuit 46 are the same as the component of the identical codes shown in drawing 1.

[0034]The amplifying circuit 56 inputs the analog picture signal S0, amplifies this analog picture signal S0 of only -3 dB, and outputs the amplified analog picture signal S56 to the selector 53. The amplifying circuit 57 inputs the analog picture signal S0, amplifies this analog picture signal S0 of only 3 dB, and outputs the amplified analog picture signal S57 to the selector 53. The amplifying circuit 58 inputs the analog picture signal S0, amplifies this analog picture signal S0 of only 6 dB, and outputs the amplified analog picture signal S58 to the selector 53. The amplifying circuit 59 inputs the analog picture signal S0, amplifies this analog picture signal S0 of only 9 dB, and outputs the amplified analog picture signal S59 to the selector 53.

[0035]The gain decision circuit 54 outputs the 2-bit selection signal S54a to the selector 53 based on the gain detecting signal S46. Based on the gain detecting signal S46, the gain decision circuit 54 specifically, When the peak level of the analog picture signal S12 is over the input dynamic range of the A/D conversion circuit 13, or when it has stuck to the maximum after an A/D conversion, the selection signal S54a which shows that the analog picture signal S56 is chosen is outputted. Based on the gain detecting signal S46, the gain decision circuit 54 the peak level of the analog picture signal S12, In being larger than $1/2^{1/2}$ twice at 1 or less time of the input dynamic range of the A/D conversion circuit 13, it outputs the selection signal S54a which shows that the analog picture signal S0 is chosen.

[0036]Based on the gain detecting signal S46, the gain decision circuit 54 the peak level of the analog picture signal S12, In being larger than 1/2 at less than the $1/2^{1/2}$ twice of the input dynamic range of the A/D conversion circuit 13, it outputs the selection signal S54a which shows that the analog picture signal S57 is chosen. Based on the gain detecting signal S46, the gain decision circuit 54 the peak level of the analog picture signal S12, In being larger than $1-/(2x2^{1/2})$ twice at 1/2 or less twice of the input dynamic range of the A/D conversion circuit 13, it outputs the selection signal S54a which shows that the analog picture signal S58 is chosen. Based on the gain detecting signal S46, the gain decision circuit 54, The peak level of the analog picture signal S12 outputs the selection signal S54a which shows that the analog picture signal S59 is chosen by below $1-/(2x2^{1/2})$ double [of the input dynamic range of the A/D conversion circuit 13].

[0037]Operation of the picture signal processing circuit 51 shown in drawing 2 is explained briefly. Operation of the picture signal processing circuit 51 is the same as the picture signal processing

circuit 41 shown in drawing 1 except for the point which chooses any or 1 of the analog picture signal S0, S56, S57, S58, and S59 in the selector 53 based on the selection signal S54a from the gain decision circuit 54.

[0038]Namely, in the gain decision circuit 54 based on the gain detecting signal S46, The selection signal S54a which shows any are chosen among the analog picture signal S0, S56, S57, S58, and S59 is outputted to the selector 53, Based on the selection signal S54a concerned, the amplified analog picture signal S56, S57, S58, S59, or the analog picture signal S0 is chosen by the selector 53, and is outputted to the pre-filter 11 as the analog picture signal S53.

[0039]It is band-limited in the pre-filter 11, bottom product potential is adjusted in the sink chip clamp circuit 12, and the A/D conversion of the analog picture signal S53 is carried out in the A/D conversion circuit 13, and it is outputted to LPF14 as the 8-bit digital image signal S13. In LPF14, a horizontal high-frequency component is removed and the digital image signal S13 turns into the digital image signal S14 which is 10 bits.

[0040]Based on the selection signal S39 which shows that the digital image signal S14 chooses the analog picture signal S32, By first, the feedback control of the digital system by the digital AGC circuit 45, LPF32, the AGC gain detector circuit 46, and the gain decision circuit 44. For example, gain control of the sink level is carried out so that it may be set to 401IRE in the case of NTSC system, and it may be set to 431IRE in the case of a PAL system. Next, the selection signal S39 switches so that choosing the analog picture signal S45 may be shown, and the digital image signal S14, Gain control is carried out so that a peak level may fill a regular range by the feedback control of the digital system by the digital AGC circuit 45, the AGC gain detector circuit 46, and the gain decision circuit 44.

[0041]As explained above, according to the picture signal processing circuit 51, by the gain decision circuit 54, the amplifying circuits 56, 57, 58, and 59, and the selector 53. Since feedback control by an analog form is finely performed compared with the picture signal processing circuit 41 shown in drawing 1, still highly precise gain control can be performed compared with the picture signal processing circuit 41.

[0042]3rd embodiment drawing 3 is a lineblock diagram of the picture signal processing circuit 61 of this embodiment. As shown in drawing 3, the picture signal processing circuit 61 is the same as the picture signal processing circuit 41 shown in drawing 1 fundamentally, but the composition of the gain decision circuit 64 differs in the gain decision circuit 44. Namely, the gain decision circuit 64 is provided with the gain judging level shift circuit 70 shown in drawing 4, To the function of the gain decision circuit 44, in addition, near the gain judging level (0.750 ****-p) used as the standard which switches the selection signal S44a, When changing the sink level or peak level shown by the gain detecting signal S46, it has the function to avoid that the switch of the selector 43 switches frequently.

[0043]Hereafter, the gain judging level shift circuit 70 is explained. As shown in drawing 4, the gain judging level shift circuit 70 has the comparison circuit 71, the field counter 72, AND circuit 73, and the level shift decision circuit 74. The comparison circuit 71 The gain detecting signal S46 from the AGC gain detector circuit 46, The level which performs comparison with a gain judging level when generating the selection signal S44a, for example, the gain detecting signal S46 shows outputs the comparison signal S71 which becomes high-level to AND circuit 73, when large compared with a gain judging level.

[0044]The field counter 72 inputs the digital image signal S32 or S45, and outputs the field detected pulse signal S72 with which only predetermined time becomes high-level to AND circuit 73 and the level shift decision circuit 74 for every field based on the Vertical Synchronizing signal included in these.

[0045]AND circuit 73 outputs the level of the comparison signal S71 when the field detected pulse signal S72 is high-level to the level shift decision circuit 74 as the operation signal S73.

[0046]The level shift decision circuit 74 counts a field number based on the field detected pulse

signal S72, and it counts the pulse number contained in the operation signal S73. The level shift decision circuit 74 obtains the frequency where it is detecting how many pulses occurring to the operation signal S73, and the selection signal S44b switches into the field of a predetermined number. And if the level shift decision circuit 74 judges that the selection signal S44b switched into the field of a predetermined number in more than the predetermined number of times, it will lower a gain judging level to 0.750-0.500V.

[0047]As explained above, according to the picture signal processing circuit 61, by using the gain judging level shift circuit 70. Even when the level which the gain detecting signal S46 shows is changed near a gain judging level, it avoids effectively that the selector 43 switches frequently, and makes it possible to be stabilized and to provide a high-definition picture.

[0048]This invention is not limited to the embodiment mentioned above. For example, the number and gain of an amplifying circuit which are shown in drawing 1 - 3 are not limited to what is shown in the embodiment mentioned above, but can be arbitrarily changed into it according to the input dynamic range and the accuracy demanded of the A/D conversion circuit 13. various circuitry of the gain judging level shift circuit 70 shown in drawing 4 can also be boiled, and can be changed. For example, the field counter 72 may not be formed but the timer etc. which measure predetermined time may be used.

[0049]Although the gain illustrated the fixed thing in the embodiment mentioned above as the amplifying circuits 42, 56, 57, 58, and 59 shown in drawing 1 - 3, a gain as shown in drawing 5 (A), (B), and (C) may use a variable amplifying circuit. In this case, according to the input dynamic range of the analog picture signal S0 and the A/D conversion circuit 13, a user adjusts the gain of an amplifying circuit. Five resistance R1 is connected in series between the input terminal 90 and the output terminal 91, and, as for the amplifying circuit shown in drawing 5 (A), the terminals 92a, 92b, 92c, and 92d are pulled out from between resistance between. The switch 94 which connects selectively the terminals 92a, 92b, 92c, and 92d and - input terminal of the operational amplifier 93 is formed. The output terminal of the operational amplifier 93 is connected to the output terminal 91. In the amplifying circuit shown in drawing 5 (A), the switch 94 is selectively connected to the terminals 92a, 92b, 92c, and 92d according to a gain. A gain becomes low as the switch 94 switches from the terminal 92a toward 92 d at this time.

[0050]The switch 104 is selectively connected to the terminals 102a, 102b, 102c, and 102d, it passes any of the resistance R3, R4, R5, and R6 they are, and, as for the amplifying circuit shown in drawing 5 (B), - input terminal and the output terminal 101 of the operational amplifier 103 are connected by this.

[0051]The switch 114 is selectively connected to the terminals 112a, 112b, 112c, and 112d, it passes any of the resistance R7, R8, R9, and R10 they are, and, as for the amplifying circuit shown in drawing 5 (C), - input terminal and the input terminal 110 of the operational amplifier 113 are connected by this.

[0052]

[Effect of the Invention]As explained above, according to the picture signal processing circuit of this invention, by small-scale circuitry, gain control can be performed with high precision and can be developed moreover comparatively easily.

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TECHNICAL FIELD

[Field of the Invention]This invention relates to a picture signal processing circuit.

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PRIOR ART

[Description of the Prior Art]For example, NTSC (National Television Committee) which received A method and PAL (Phase Alternation by Line) To the decoder of the receiving set which carries out digital processing, the analog picture signal of a method usually, A (Analog)/D (Digital) which changes the received analog picture signal into digital image data The conversion circuit is built in. If the electric wave induced by the antenna has strength for example, the received analog picture signal will be changed similarly and the contrast of a screen, etc. will change. In order to use as a predetermined level the level of the analog picture signal received to the decoder of the receiving set in order to avoid this, the AGC (Automatic Gain Control) circuit which controls a gain is built in.
[0003]The picture signal processing circuit hereafter provided with the A/D conversion circuit and AGC circuit which were built in the decoder of the conventional receiving set is explained. Drawing 6 is the lineblock diagram of the picture signal processing circuit 1 which performs gain detection with an analog form and performs gain control with an analog form built in the decoder of the conventional receiving set. In the picture signal processing circuit 1, the analog picture signals S0, such as a luminance signal, a composite signal, or a chrominance signal, are inputted, and the gain control amplifier 10 performs gain control for this analog picture signal S0 based on the gain detecting signal S16 from the AGC gain detector circuit 16. The analog picture signal S10 from the gain control amplifier 10 is outputted to the low pass filter (LPF) 15, the AGC gain detector circuit 16, and the pre-filter 11.
[0004]Horizontal high-frequency components, such as a subcarrier, are removed by the low pass filter 15, and, as for the analog picture signal S10, the analog picture signal S15 restricted to 1 MHz is outputted for a zone to the AGC gain detector circuit 16. the synchronized signal with which the analog picture signal S15 is included in the analog picture signal S0 here -- abbreviated -- it is the same. In the AGC gain detector circuit 16, gain detection is selectively performed based on the selection signal S19 about the analog picture signal S15 from the low pass filter 15, and the analog picture signal S10 from the gain conte row amplifier 10, The gain control signal S16 according to the gain detection concerned is outputted to the gain control amplifier 10.
[0005]Specifically in the AGC gain detector circuit 16. When the analog picture signal S15 is chosen, gain detection is performed about the synchronized signal contained in the analog picture signal S0, and feedback gain control is performed about the synchronized signal concerned in the gain control amplifier 10. For example, feedback gain control is performed so that the gain of a synchronized signal may become with 401IRE in the case of NTSC system and may become with 431IRE in the case of a PAL system.
[0006]On the other hand, in the AGC gain detector circuit 16, when the analog picture signal S10 is chosen, in the gain control amplifier 10 and the AGC gain detector circuit 16, gain control is performed about the signal of all the zones included in the analog picture signal S0. That is, feedback gain control is performed so that the peak level of the analog picture signal S0 may be settled in a predetermined range. For example, as the input dynamic ranges in the A/D conversion

circuit 13 are 1.500 ****-p and it is shown in drawing 7 and drawing 8, When the peak level of the 100% of analog image color bar signal S0 is as low as 1.243V and 0.621V, the gain control amplifier 10 performs gain control so that a peak level may generate the analog picture signal S10 used as 1.434V. As shown in drawing 9, when the peak level of the 100% of analog image color bar signal S0 is as high as 1.912V, the gain control amplifier 10 performs gain control so that a peak level may generate the analog picture signal S10 used as 1.434V.

[0007]The analog picture signal S10 is band-limited in the pre-filter 11 so that aliasing may not arise at the time of the A/D conversion in the latter A/D conversion circuit 13. This band-limited analog picture signal S11 is adjusted to bottom product potential [in / in that bottom product potential / the A/D conversion circuit 13] in the sink chip clamp circuit 12. In [in the A/D conversion circuit 13, the A/D conversion of the analog picture signal S12 is carried out by the quantization step according to the reference signal S18, and] LPF14 this 8-bit digital image signal S13, A horizontal high-frequency component is removed, for example, it becomes the digital image signal S14 which is 10 bits.

[0008]Drawing 10 is the lineblock diagram of the picture signal processing circuit 21 which performs gain detection with a digital system and performs gain control with an analog form built in the decoder of the conventional receiving set. In the picture signal processing circuit 21, the digital image signal S14 from LPF14 is outputted to LPF22 and the AGC gain detector circuit 26. In LPF22, horizontal high-frequency components, such as a subcarrier, are removed, a zone is restricted to 1 MHz, and the digital image signal S14 turns into the digital image signal S22. The digital image signal S22 is equivalent to what carried out the A/D conversion of the synchronized signal contained in the analog picture signal S0. In the AGC gain detector circuit 26, gain detection is selectively performed based on the selection signal S29 about the digital image signal S14 from the digital image signals S22 and LPF14 from the low pass filter 22, The digital gain control signal S26 according to the gain detection concerned is outputted to the D/A conversion circuit 23. D/A conversion of the gain control signal S26 is carried out to the gain control signal S23 of an analog in the D/A conversion circuit 23. Based on the gain control signal S23, feedback gain control of the analog picture signal S0 is carried out in the gain control amplifier 20.

[0009]Drawing 11 is the lineblock diagram of the picture signal processing circuit 31 which performs gain detection with a digital system and performs gain control with a digital system built in the decoder of the conventional receiving set. The analog picture signal S0 is processed in pre-filter 11, sink chip clamp circuit 12, A/D conversion circuit 13, and LPF14, and is inputted into digital AGC30 as the digital image signal S14. Based on the gain control signal S33 of digital format, feedback gain control is carried out and the digital image signal S14 is outputted as the digital image signal S30. The digital image signal S30 is outputted to LPF32 and the AGC gain detector circuit 33. About the digital image signal S32 and the digital image signal S30 corresponding to a synchronized signal, based on the selection signal S39, the AGC gain detector circuit 33 performs gain detection selectively, and outputs the gain control signal S33 according to the detection result concerned to digital AGC30.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention]As explained above, according to the picture signal processing circuit of this invention, by small-scale circuitry, gain control can be performed with high precision and can be developed moreover comparatively easily.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]However, in the picture signal processing circuit 1 shown in drawing 6 mentioned above. Since feedback control of the gain control amplifier 10 is carried out by the analog form with the gain control signal S16 from the AGC gain detector circuit 16, it is difficult to realize linear gain control, and development time will delay. It is not easy to design the circuit in which the transistor of CMOS which constitutes the gain control amplifier 10 specifically has the desired characteristic.
[0011]In the picture signal processing circuit 21 shown in drawing 10 mentioned above, since the gain control signal S26 is generated by digital format in the AGC gain detector circuit 26, can perform gain control with high precision, but. Since the D/A conversion circuit 23 is generally formed, there is a problem that a circuit will large-scale-ize.
[0012]In the picture signal processing circuit 31 shown in drawing 11 mentioned above. Since gain control is performed by digital format after an A/D conversion, when the amplitude of the analog picture signal S0 is small, The A/D conversion fully using the input dynamic range of the A/D conversion circuit 13 will not be able to be performed, but quantization will become rude, and image quality deterioration will be an intense dirty picture under the influence of a quantization noise.
[0013]This invention is made in view of the conventional technology mentioned above, is small-scale circuitry, and can perform gain control with high precision, and an object of this invention is to provide comparatively simply the picture signal processing circuit which can be developed.

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MEANS

[Means for Solving the Problem]In order to solve a problem of conventional technology mentioned above and to attain the purpose mentioned above, a picture signal processing circuit of this invention is provided with the following.
The singular number which amplifies an inputted analog picture signal by a predetermined gain, or two or more amplifying means.
A selecting means which chooses an analog picture signal of 1 from two or more analog picture signals based on a selection signal for analog picture signal selection among said inputted analog picture signal and said amplified analog picture signal.
An analog-to-digital conversion means to change said selected analog picture signal into digital image data.
A level adjustment means to adjust a level of said digital image signal by a gain according to a control signal, A gain detection means to detect a gain of said digital image signal by which level adjustment was carried out, and a gain judging means which generates a selection signal and said control signal for said analog picture signal selection based on said detected gain.

[0015]A picture signal processing circuit of this invention determines then an analog picture signal chosen in a selecting means in a gain judging means based on a gain detection result. Therefore, based on a gain detection result, an amplification factor of an inputted analog picture signal can be determined, and an inputted analog picture signal can be amplified so that an input dynamic range of processing may be efficiently used at the time of conversion in an analog-to-digital conversion means. In a gain judging means, since a level adjustment means of a digital system is controlled based on a gain detected by a gain detection means, a digital system can perform highly precise level adjustment (AGC), i.e., automatic gain control.
[0016]
[Embodiment of the Invention]Hereafter, the picture signal processing circuit concerning the embodiment of this invention is explained. In the conventional picture signal processing circuit, when carrying out the A/D conversion of the analog picture signals, such as NTSC system or a PAL system, The both sides of an analog form and a digital system perform double feedback control in the picture signal processing circuit of this embodiment to having performed gain control by either one of the analog form or the digital system.
[0017]1st embodiment drawing 1 is a lineblock diagram of the picture signal processing circuit 41 of this embodiment. As shown in drawing 1, the picture signal processing circuit 41 is provided with the amplifying circuit 42, the selector 43, the pre-filter 11, the sink chip clamp circuit 12, the A/D conversion circuit 13, LPF14, the digital AGC circuit 45, LPF32, the AGC gain detector circuit 46, and the gain decision circuit 44. Here, the pre-filter 11, the sink chip clamp circuit 12, and the A/D conversion circuit 13 are the same as the component of the identical codes of the picture signal processing circuit 1 shown in drawing 5. LPF32 is the same as the component of the identical codes

of the picture signal processing circuit 31 shown in drawing 10. The picture signal processing circuit 41 is built in the decoder of the receiving set which carries out digital processing of the analog picture signal of the NTSC system and the PAL system which were received, for example.
[0018]The amplifying circuit 42 inputs the analog picture signals S0, such as a luminance signal, a composite signal, or a chrominance signal, amplifies this analog picture signal S0 of only 6 dB, and outputs the amplified analog picture signal S42 to the input terminal 43b of the selector 43. Based on the selection signal S44a from the gain decision circuit 44 (for example, 1 bit), the selector 43 switches the switch 43c between the input terminal S43a and S43b, and outputs selectively the analog picture signal S0 or S42 to the pre-filter 11 as the analog picture signal S43.
[0019]The pre-filter 11 performs filtering to the analog picture signal S43, and restricts frequency to a predetermined zone so that aliasing may not occur at the time of an A/D conversion. The sink chip clamp circuit 12 adjusts the bottom product potential of the analog picture signal S11 from the pre-filter 11 to the bottom product potential in the A/D conversion in the A/D conversion circuit 13, and outputs this adjusted analog picture signal S12 to the A/D conversion circuit 13.
[0020]The A/D conversion circuit 13 carries out the A/D conversion of the analog picture signal S12 by the quantization step according to the reference signal S18, and outputs the 8-bit digital image signal S13 to LPF14. To the digital image signal S13, LPF14 performs filtering, and removes a horizontal broader-based ingredient, for example, outputs the 10-bit digital image signal S14 to the digital AGC circuit 45.
[0021]Based on the gain control signal S44b from the gain decision circuit 44, the digital AGC circuit 45 performs feedback gain control of a digital system to the digital image signal S14, and outputs the digital image signal S45 concerned by which gain control was carried out. LPF32 removes horizontal high-frequency components, such as a subcarrier, to the digital image signal S45 from the digital AGC circuit 45, and a zone outputs the digital image signal S32 restricted to about 1 MHz to the AGC gain detector circuit 46. The digital image signal S32 is a digital signal corresponding to the synchronized signal contained in the analog picture signal S0.
[0022]According to the selection signal S39, the AGC gain detector circuit 46 about the digital image signal S32 from LPF32, and the digital image signal S45 from the digital AGC circuit 45. Selectively, a digital system performs gain detection and the gain detecting signal S46 according to the detection result concerned is outputted to the gain decision circuit 44. When the selection signal S39 is pointing to detection of the sink level, the AGC gain detector circuit 46 performs gain detection of the digital image signal S32, and, specifically, detects the sink level of the synchronized signal contained in the digital image signal S45. On the other hand, when the selection signal S39 is pointing to detection of the Max level, the AGC gain detector circuit 46 performs gain detection of the digital image signal S45, and detects the peak level of the digital image signal S45. For example, a peak level can be adjusted after adjusting the sink level of the digital image signal S45 in the digital AGC circuit 45 by making it direct detection of the Max level after the selection signal S39 points to detection of a sink level.
[0023]The gain decision circuit 44 receives the amplitude of the analog picture signal S12 based on the gain detecting signal S46, When it judges whether the input dynamic range of the A/D conversion circuit 13 is generous and it is judged that it is generous, the selection signal S44a which shows that it switches to the input terminal 43b is outputted to the selector 43. Here, the input dynamic ranges of the A/D conversion circuit 13 are 0-1.500V, for example. On the other hand, the gain decision circuit 44 outputs the selection signal S44a with which ****** shows that it switches to the input terminal 43a at a case if a margin does not have an input dynamic range of the A/D conversion circuit 13 to the amplitude of the analog picture signal S12 at the selector 43. Based on the gain detecting signal S46, when the peak level of the analog picture signal S12 is below half of the input dynamic range of the A/D conversion circuit 13, it specifically judges that it is generous, and in being larger than a half, it judges that it is hard-pressed.
[0024]The gain decision circuit 44 generates the gain control signal S44b for carrying out feedback

gain control of the digital image signal S45 in the digital AGC circuit 45 at a predetermined level based on the gain detecting signal S46, and outputs this to the digital AGC circuit 45.
[0025]Hereafter, operation of the picture signal processing circuit 41 shown in drawing 1 is explained. First, the peak of the amplitude of the analog picture signal S0 explains the case where it is below half (0.750V) of the input dynamic range (1.500V) of the A/D conversion circuit 13. In this case, in the gain decision circuit 44 based on the gain detecting signal S46, The selection signal S44a which shows that a switch is switched to the input terminal 43b is outputted to the selector 43, and the analog picture signal S42 which amplified the analog picture signal S0 of only 6 dB is outputted to the pre-filter 11 as the analog picture signal S43. That is, the analog picture signal S43 which doubled the amplitude of the analog picture signal S0 is outputted to the pre-filter 11.
[0026]It is band-limited in the pre-filter 11, bottom product potential is adjusted in the sink chip clamp circuit 12, and the A/D conversion of the analog picture signal S43 is carried out in the A/D conversion circuit 13, and it is outputted to LPF14 as the 8-bit digital image signal S13. In LPF14, a horizontal high-frequency component is removed and the digital image signal S13 turns into the digital image signal S14 which is 10 bits. Based on the selection signal S39 which shows that the digital image signal S14 chooses the analog picture signal S32, By first, the feedback control of the digital system by the digital AGC circuit 45, LPF32, the AGC gain detector circuit 46, and the gain decision circuit 44. For example, gain control of the sink level is carried out so that it may be set to 401IRE in the case of NTSC system, and it may be set to 431IRE in the case of a PAL system.
Next, the selection signal S39 switches so that choosing the analog picture signal S45 may be shown, and the digital image signal S14, Gain control is carried out so that a peak level may fill a regular range by the feedback control of the digital system by the digital AGC circuit 45, the AGC gain detector circuit 46, and the gain decision circuit 44.
[0027]Next, the peak of the amplitude of the analog picture signal S0 explains the case where it is larger than the half (0.750V) of the input dynamic range (1.500V) of the A/D conversion circuit 13. In this case, based on the gain detecting signal S46, in the gain decision circuit 44, the selection signal S44a which shows that a switch is switched to the input terminal 43a is outputted to the selector 43, and the analog picture signal S0 is outputted to the pre-filter 11 as the analog picture signal S43.
[0028]It is band-limited in the pre-filter 11, bottom product potential is adjusted in the sink chip clamp circuit 12, and the A/D conversion of the analog picture signal S43 is carried out in the A/D conversion circuit 13, and it is outputted to LPF14 as the 8-bit digital image signal S13. In LPF14, a horizontal high-frequency component is removed and the digital image signal S13 turns into the digital image signal S14 which is 10 bits. Subsequent processing is the same as the case where the peak of the amplitude of the analog picture signal S0 mentioned above is below half (0.750V) of an input dynamic range (1.500V).
[0029]As explained above, since feedback control of the gain of the digital image signal S14 is carried out with a digital system, highly precise gain control can be performed in the picture signal processing circuit 41 by the digital AGC circuit 45, the AGC gain detector circuit 46, and the gain decision circuit 44. That is, according to the picture signal processing circuit 41, the quality digital image signal acquired by carrying out the A/D conversion of the analog picture signal S0 of NTSC system or a PAL system can be outputted to a latter digital signal processing circuit. In the picture signal processing circuit 41, below half of the input dynamic range of the A/D conversion circuit 13 outputs the analog picture signal S12 which amplified the amplitude of the analog picture signal S0 twice to the A/D conversion circuit 13, when the amplitude of the peak level of the analog picture signal S0 is very low. Therefore, it can avoid effectively that quantization precision becomes rude to the analog picture signal S0 with a low peak level of amplitude like the picture signal processing circuit 31 shown in drawing 10 mentioned above, and the influence of a quantization noise can be reduced.
[0030]In order that giving the desired characteristic like the picture signal processing circuit 1

shown in drawing 5 only with outputting the several bits selection signal S44a to the selector 43 may not perform gain control of a difficult analog form according to the picture signal processing circuit 41, a circuit design is easy and a development cycle is also short.

[0031]Like the picture signal processing circuit 21 shown in drawing 9, since a D/A conversion circuit is not used, small-scale circuitry is realizable in the picture signal processing circuit 41.

[0032]Namely, according to the picture signal processing circuit 41, the analog picture signal S0 is received, The gain decision circuit 44, the amplifying circuit 42, and the selector 43 perform rude gain control by an analog form, After an A/D conversion, by performing gain control finely with a digital system by the digital AGC circuit 45, the AGC gain detector circuit 46, and the gain decision circuit 44. Highly precise gain control with little influence of a quantization noise can be performed, a circuit design is easy, a development cycle is short, and, moreover, a circuit can be made comparatively small-scale.

[0033]2nd embodiment drawing 2 is a lineblock diagram of the picture signal processing circuit 51 of this embodiment. As shown in drawing 2, the picture signal processing circuit 51, It has the amplifying circuits 56, 57, 58, and 59, the selector 53, the pre-filter 11, the sink chip clamp circuit 12, the A/D conversion circuit 13, the column decoder 14, the digital AGC circuit 45, LPF32, the AGC gain detector circuit 46, and the gain decision circuit 54. Here, the pre-filter 11 shown in drawing 2, the sink chip clamp circuit 12, the A/D conversion circuit 13, the column decoder 14, the digital AGC circuit 45, LPF32, and the AGC gain detector circuit 46 are the same as the component of the identical codes shown in drawing 1.

[0034]The amplifying circuit 56 inputs the analog picture signal S0, amplifies this analog picture signal S0 of only -3 dB, and outputs the amplified analog picture signal S56 to the selector 53. The amplifying circuit 57 inputs the analog picture signal S0, amplifies this analog picture signal S0 of only 3 dB, and outputs the amplified analog picture signal S57 to the selector 53. The amplifying circuit 58 inputs the analog picture signal S0, amplifies this analog picture signal S0 of only 6 dB, and outputs the amplified analog picture signal S58 to the selector 53. The amplifying circuit 59 inputs the analog picture signal S0, amplifies this analog picture signal S0 of only 9 dB, and outputs the amplified analog picture signal S59 to the selector 53.

[0035]The gain decision circuit 54 outputs the 2-bit selection signal S54a to the selector 53 based on the gain detecting signal S46. Based on the gain detecting signal S46, the gain decision circuit 54 specifically, When the peak level of the analog picture signal S12 is over the input dynamic range of the A/D conversion circuit 13, or when it has stuck to the maximum after an A/D conversion, the selection signal S54a which shows that the analog picture signal S56 is chosen is outputted. Based on the gain detecting signal S46, the gain decision circuit 54 the peak level of the analog picture signal S12, In being larger than $1/2^{1/2}$ twice at 1 or less time of the input dynamic range of the A/D conversion circuit 13, it outputs the selection signal S54a which shows that the analog picture signal S0 is chosen.

[0036]Based on the gain detecting signal S46, the gain decision circuit 54 the peak level of the analog picture signal S12, In being larger than 1/2 at less than the $1/2^{1/2}$ twice of the input dynamic range of the A/D conversion circuit 13, it outputs the selection signal S54a which shows that the analog picture signal S57 is chosen. Based on the gain detecting signal S46, the gain decision circuit 54 the peak level of the analog picture signal S12, In being larger than $1-/(2x2^{1/2})$ twice at 1/2 or less twice of the input dynamic range of the A/D conversion circuit 13, it outputs the selection signal S54a which shows that the analog picture signal S58 is chosen. Based on the gain detecting signal S46, the gain decision circuit 54, The peak level of the analog picture signal S12 outputs the selection signal S54a which shows that the analog picture signal S59 is chosen by below $1-/(2x2^{1/2})$ double [of the input dynamic range of the A/D conversion circuit 13].

[0037]Operation of the picture signal processing circuit 51 shown in drawing 2 is explained briefly. Operation of the picture signal processing circuit 51 is the same as the picture signal processing

circuit 41 shown in drawing 1 except for the point which chooses any or 1 of the analog picture signal S0, S56, S57, S58, and S59 in the selector 53 based on the selection signal S54a from the gain decision circuit 54.

[0038]Namely, in the gain decision circuit 54 based on the gain detecting signal S46, The selection signal S54a which shows any are chosen among the analog picture signal S0, S56, S57, S58, and S59 is outputted to the selector 53, Based on the selection signal S54a concerned, the amplified analog picture signal S56, S57, S58, S59, or the analog picture signal S0 is chosen by the selector 53, and is outputted to the pre-filter 11 as the analog picture signal S53.

[0039]It is band-limited in the pre-filter 11, bottom product potential is adjusted in the sink chip clamp circuit 12, and the A/D conversion of the analog picture signal S53 is carried out in the A/D conversion circuit 13, and it is outputted to LPF14 as the 8-bit digital image signal S13. In LPF14, a horizontal high-frequency component is removed and the digital image signal S13 turns into the digital image signal S14 which is 10 bits.

[0040]Based on the selection signal S39 which shows that the digital image signal S14 chooses the analog picture signal S32, By first, the feedback control of the digital system by the digital AGC circuit 45, LPF32, the AGC gain detector circuit 46, and the gain decision circuit 44. For example, gain control of the sink level is carried out so that it may be set to 401IRE in the case of NTSC system, and it may be set to 431IRE in the case of a PAL system. Next, the selection signal S39 switches so that choosing the analog picture signal S45 may be shown, and the digital image signal S14, Gain control is carried out so that a peak level may fill a regular range by the feedback control of the digital system by the digital AGC circuit 45, the AGC gain detector circuit 46, and the gain decision circuit 44.

[0041]As explained above, according to the picture signal processing circuit 51, by the gain decision circuit 54, the amplifying circuits 56, 57, 58, and 59, and the selector 53. Since feedback control by an analog form is finely performed compared with the picture signal processing circuit 41 shown in drawing 1, still highly precise gain control can be performed compared with the picture signal processing circuit 41.

[0042]3rd embodiment drawing 3 is a lineblock diagram of the picture signal processing circuit 61 of this embodiment. As shown in drawing 3, the picture signal processing circuit 61 is the same as the picture signal processing circuit 41 shown in drawing 1 fundamentally, but the composition of the gain decision circuit 64 differs in the gain decision circuit 44. Namely, the gain decision circuit 64 is provided with the gain judging level shift circuit 70 shown in drawing 4, To the function of the gain decision circuit 44, in addition, near the gain judging level (0.750 ****-p) used as the standard which switches the selection signal S44a, When changing the sink level or peak level shown by the gain detecting signal S46, it has the function to avoid that the switch of the selector 43 switches frequently.

[0043]Hereafter, the gain judging level shift circuit 70 is explained. As shown in drawing 4, the gain judging level shift circuit 70 has the comparison circuit 71, the field counter 72, AND circuit 73, and the level shift decision circuit 74. The comparison circuit 71 The gain detecting signal S46 from the AGC gain detector circuit 46, The level which performs comparison with a gain judging level when generating the selection signal S44a, for example, the gain detecting signal S46 shows outputs the comparison signal S71 which becomes high-level to AND circuit 73, when large compared with a gain judging level.

[0044]The field counter 72 inputs the digital image signal S32 or S45, and outputs the field detected pulse signal S72 with which only predetermined time becomes high-level to AND circuit 73 and the level shift decision circuit 74 for every field based on the Vertical Synchronizing signal included in these.

[0045]AND circuit 73 outputs the level of the comparison signal S71 when the field detected pulse signal S72 is high-level to the level shift decision circuit 74 as the operation signal S73.

[0046]The level shift decision circuit 74 counts a field number based on the field detected pulse

signal S72, and it counts the pulse number contained in the operation signal S73. The level shift decision circuit 74 obtains the frequency where it is detecting how many pulses occurring to the operation signal S73, and the selection signal S44b switches into the field of a predetermined number. And if the level shift decision circuit 74 judges that the selection signal S44b switched into the field of a predetermined number in more than the predetermined number of times, it will lower a gain judging level to 0.750-0.500V.

[0047]As explained above, according to the picture signal processing circuit 61, by using the gain judging level shift circuit 70. Even when the level which the gain detecting signal S46 shows is changed near a gain judging level, it avoids effectively that the selector 43 switches frequently, and makes it possible to be stabilized and to provide a high-definition picture.

[0048]This invention is not limited to the embodiment mentioned above. For example, the number and gain of an amplifying circuit which are shown in drawing 1 - 3 are not limited to what is shown in the embodiment mentioned above, but can be arbitrarily changed into it according to the input dynamic range and the accuracy demanded of the A/D conversion circuit 13. various circuitry of the gain judging level shift circuit 70 shown in drawing 4 can also be boiled, and can be changed. For example, the field counter 72 may not be formed but the timer etc. which measure predetermined time may be used.

[0049]Although the gain illustrated the fixed thing in the embodiment mentioned above as the amplifying circuits 42, 56, 57, 58, and 59 shown in drawing 1 - 3, a gain as shown in drawing 5 (A), (B), and (C) may use a variable amplifying circuit. In this case, according to the input dynamic range of the analog picture signal S0 and the A/D conversion circuit 13, a user adjusts the gain of an amplifying circuit. Five resistance R1 is connected in series between the input terminal 90 and the output terminal 91, and, as for the amplifying circuit shown in drawing 5 (A), the terminals 92a, 92b, 92c, and 92d are pulled out from between resistance between. The switch 94 which connects selectively the terminals 92a, 92b, 92c, and 92d and - input terminal of the operational amplifier 93 is formed. The output terminal of the operational amplifier 93 is connected to the output terminal 91. In the amplifying circuit shown in drawing 5 (A), the switch 94 is selectively connected to the terminals 92a, 92b, 92c, and 92d according to a gain. A gain becomes low as the switch 94 switches from the terminal 92a toward 92 d at this time.

[0050]The switch 104 is selectively connected to the terminals 102a, 102b, 102c, and 102d, it passes any of the resistance R3, R4, R5, and R6 they are, and, as for the amplifying circuit shown in drawing 5 (B), - input terminal and the output terminal 101 of the operational amplifier 103 are connected by this.

[0051]The switch 114 is selectively connected to the terminals 112a, 112b, 112c, and 112d, it passes any of the resistance R7, R8, R9, and R10 they are, and, as for the amplifying circuit shown in drawing 5 (C), - input terminal and the input terminal 110 of the operational amplifier 113 are connected by this.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]Drawing 1 is a lineblock diagram of the picture signal processing circuit concerning a 1st embodiment of this invention.
[Drawing 2]Drawing 2 is a lineblock diagram of the picture signal processing circuit concerning a 2nd embodiment of this invention.
[Drawing 3]Drawing 3 is a lineblock diagram of the picture signal processing circuit concerning a 3rd embodiment of this invention.
[Drawing 4]Drawing 4 is a lineblock diagram of the gain judging level shift circuit with which the gain decision circuit shown in drawing 3 was equipped.
[Drawing 5]Drawing 5 is a variable gain amplifying circuit which can be used as an amplifying circuit shown in drawing 1 - 3.
[Drawing 6]Drawing 6 is the lineblock diagram of the picture signal processing circuit which performs gain detection with an analog form and performs gain control with an analog form built in the decoder of the conventional receiving set.
[Drawing 7]Drawing 7 is a figure for explaining the gain control in the picture signal processing circuit shown in drawing 6.
[Drawing 8]Drawing 8 is a figure for explaining the gain control in the picture signal processing circuit shown in drawing 6.
[Drawing 9]Drawing 9 is a figure for explaining the gain control in the picture signal processing circuit shown in drawing 6.
[Drawing 10]Drawing 10 is the lineblock diagram of the picture signal processing circuit which performs gain detection with a digital system and performs gain control with an analog form built in the decoder of the conventional receiving set.
[Drawing 11]Drawing 11 is the lineblock diagram of the picture signal processing circuit which performs gain detection with a digital system and performs gain control with a digital system built in the decoder of the conventional receiving set.
[Description of Notations]
11 [-- LPF, 44 54, 64 / -- A gain decision circuit, 46 / -- An AGC gain detector circuit, 42 56, 57 58, 59 / -- An amplifying circuit, 43 53 / -- Selector] -- A pre-filter, 12 -- A sink chip clamp circuit, 13 -- An A/D conversion circuit, 14, 32

[Translation done.]

* NOTICES *

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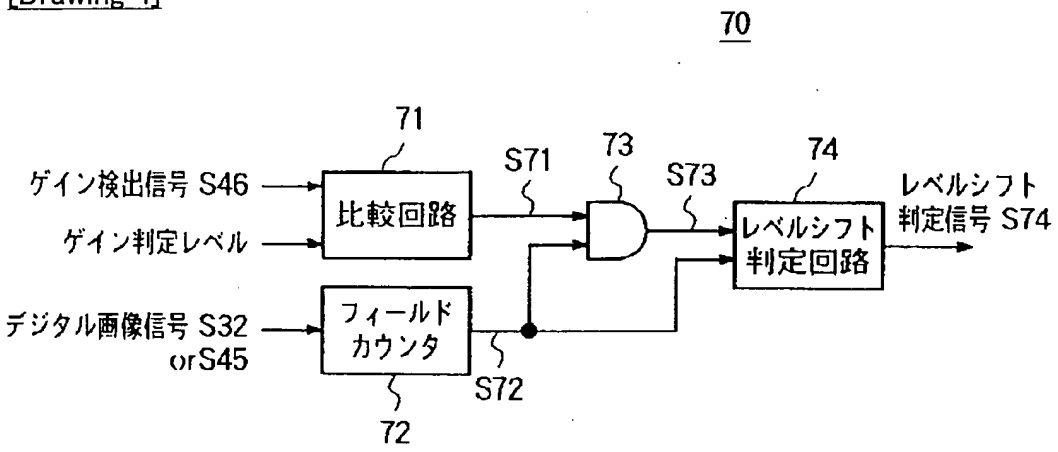
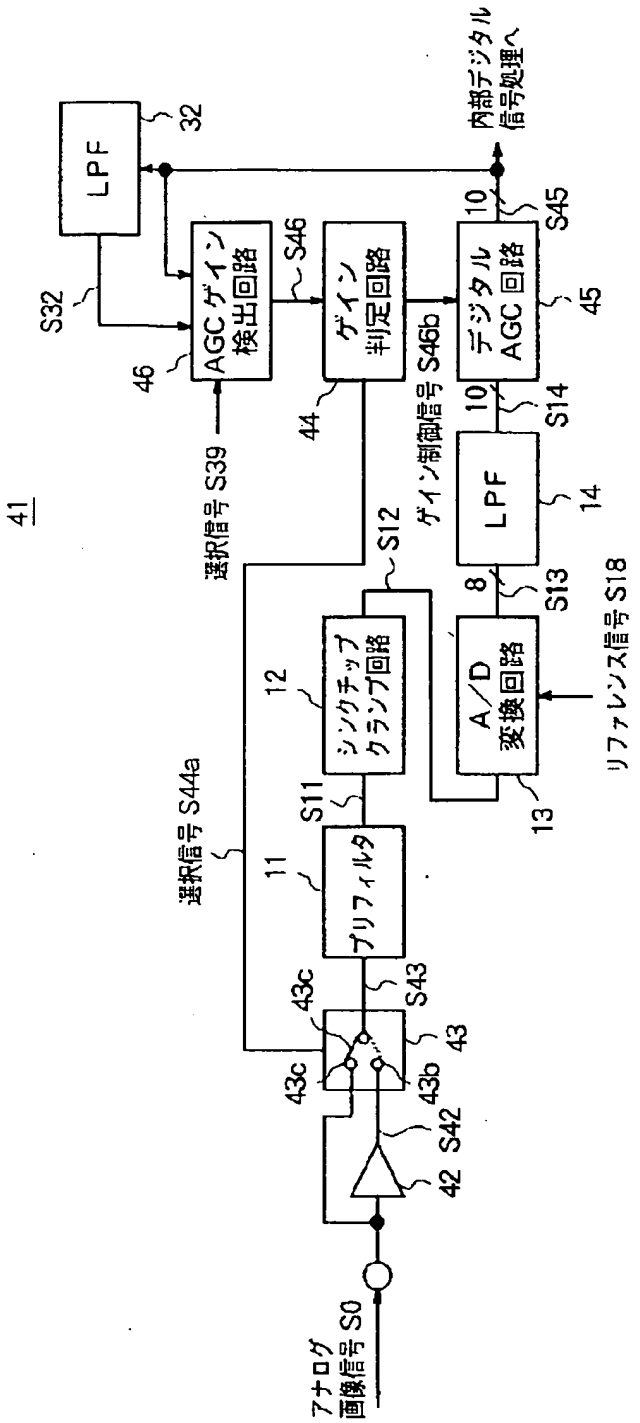
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

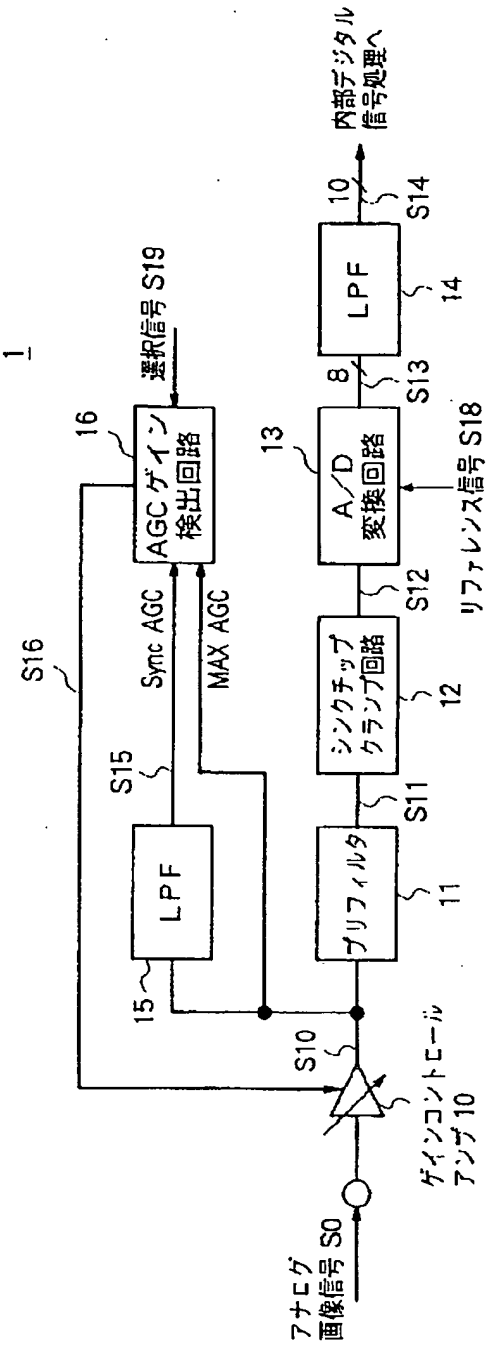
[Drawing 4]



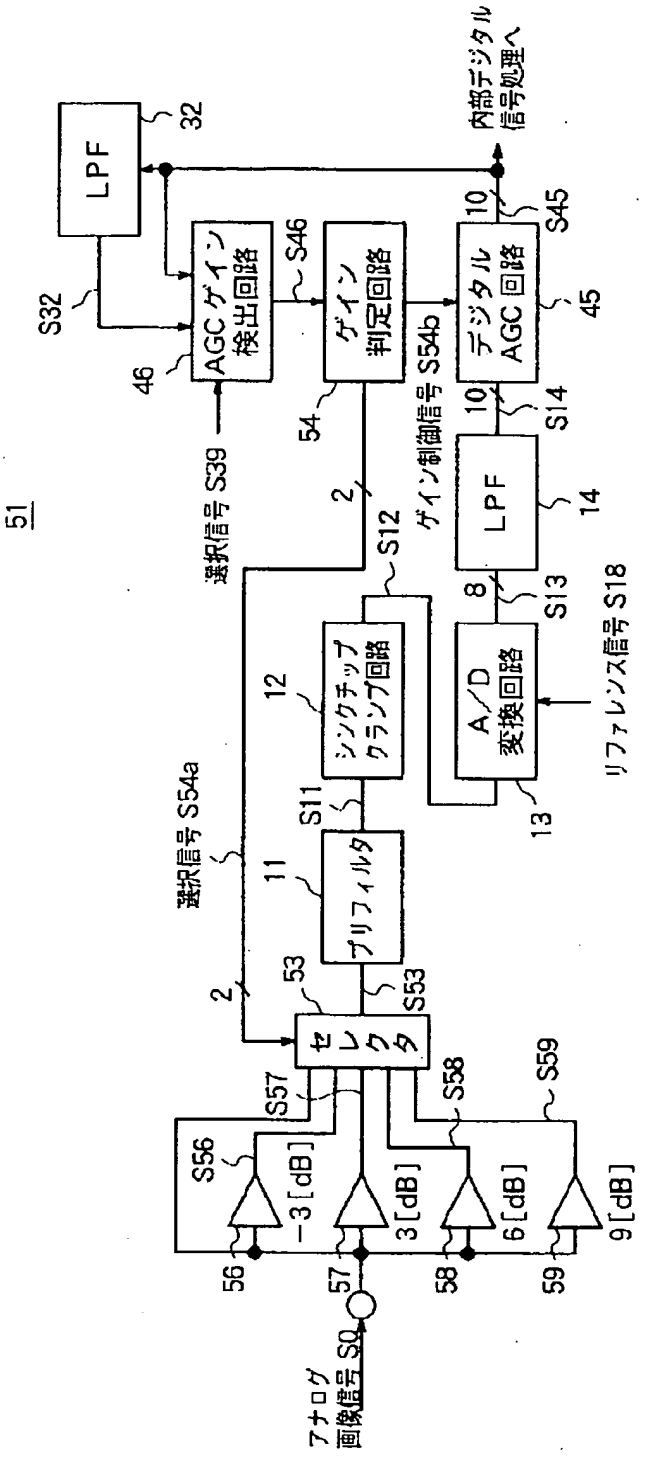
[Drawing 1]


41
LPF
32
内部デジタル信号処理へ
S32
AGCゲイン検出回路
S46
ゲイン判定回路
S45
デジタルAGC回路
46
45
10
選択信号 S39
44
ゲイン制御信号 S46b
S14
LPF
14
S12
8
S13
シンクチップクランプ回路
A/D変換回路
12
リファレンス信号 S18
S11
13
選択信号 S44a
11
プリフィルタ
43c
S43
43
43c
43b
S42
42
アナログ画像信号 S0

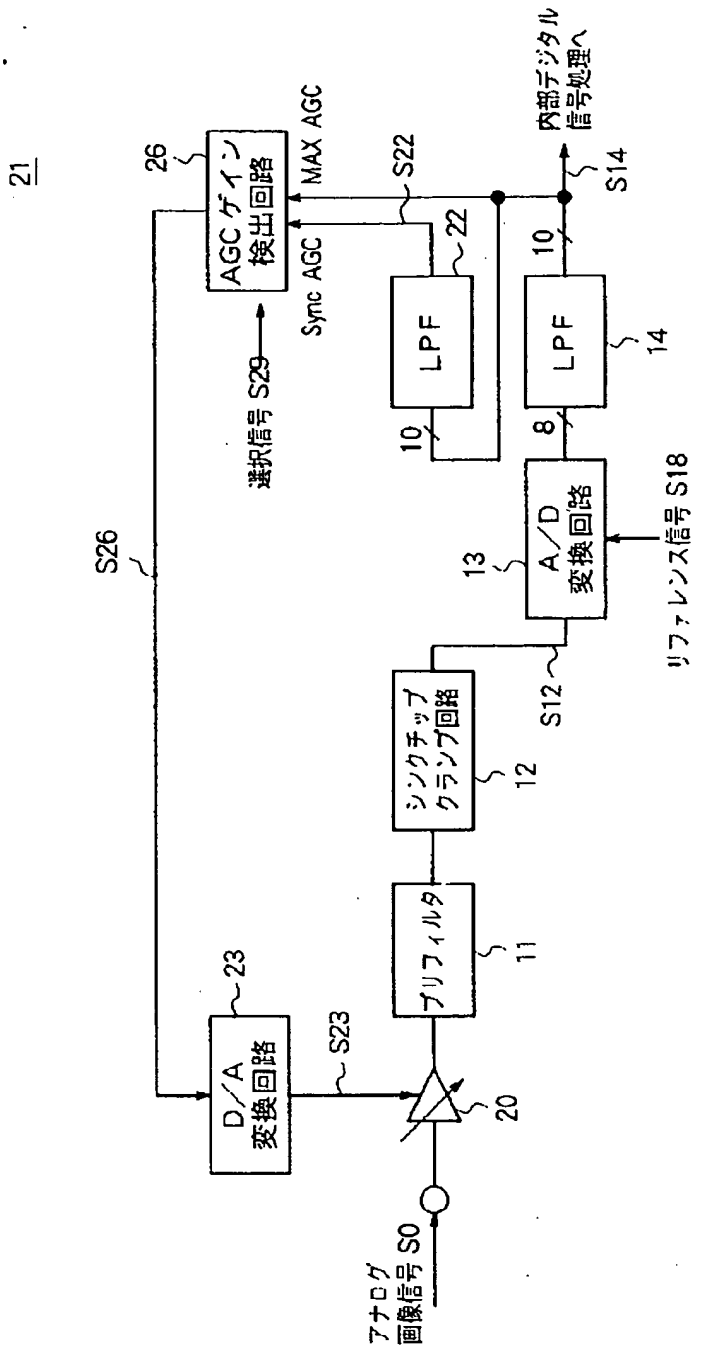
[Drawing 6]


1
アナログ画像信号 S0
ゲインコントロールアンプ 10
S10
15
LPF
S15
S16
16
AGCゲイン検出回路
選択信号 S19
Sync AGC
MAX AGC
11
プリフィルタ
S11
12
シンクチップクランプ回路
S12
13
A/D変換回路
リファレンス信号 S18
8
S13
14
LPF
10
S14
内部デジタル信号処理へ

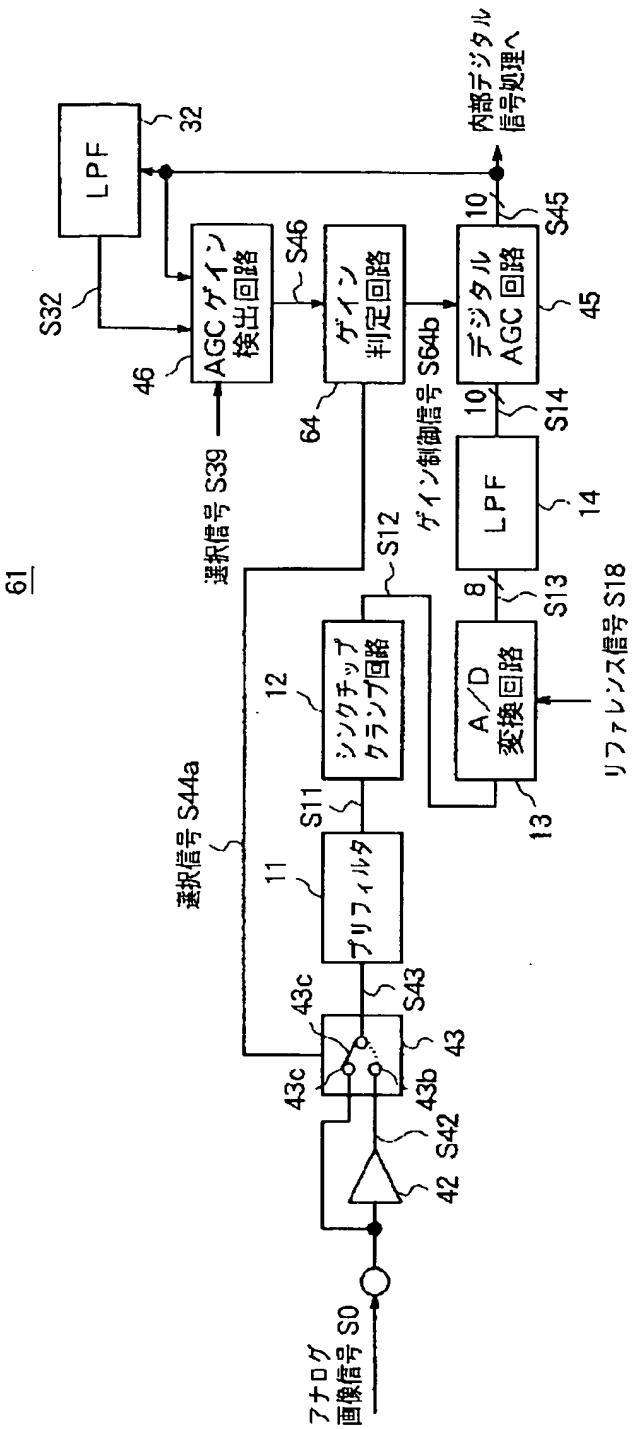
[Drawing 2]


51
LPF
32
内部デジタル信号処理へ
S32
AGCゲイン検出回路
S46
ゲイン判定回路
デジタルAGC回路
45
S45
46
54
10
S14
ゲイン制御信号 S54b
選択信号 S39
2
S12
LPF
14
8
S13
シンクチップクランプ回路
12
A/D変換回路
リファレンス信号 S18
13
S11
選択信号 S54a
11
プリフィルタ
2
53
S53
セレクタ
S57
S58
S59
S56
−3[dB]
3[dB]
6[dB]
9[dB]
56
57
58
59
アナログ画像信号 S0

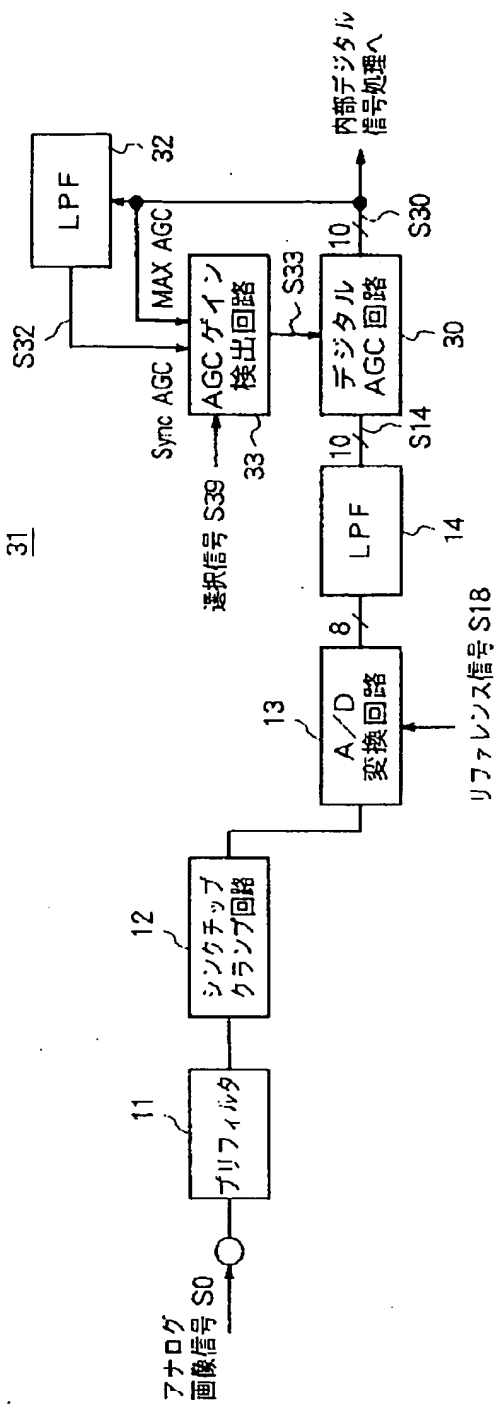
[Drawing 10]


21
26
AGC ゲイン 検出回路
MAX AGC
Sync AGC
S22
22
内部デジタル 信号処理へ
S14
10
LPF
14
選択信号 S29
10
8
A/D 変換回路
13
S26
リファレンス信号 S18
シンクチップ クランプ回路
12
S12
プリフィルタ
11
23
D/A 変換回路
S23
20
アナログ 画像信号 S0

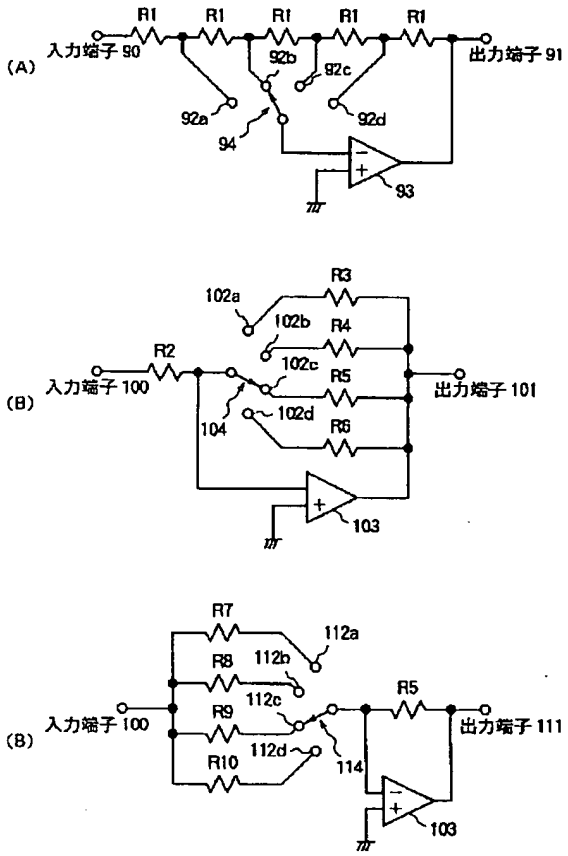
[Drawing 3]


61
LPF
32
内部デジタル信号処理へ
S32
AGCゲイン検出回路
S46
ゲイン判定回路
デジタルAGC回路
10
S45
45
46
選択信号 S39
64
ゲイン制御信号 S64b
10
S14
LPF
14
S12
8
S13
シンクチップクランプ回路
12
A/D変換回路
リファレンス信号 S18
選択信号 S44a
S11
13
プリフィルタ
11
43c
S43
43
43c
43b
S42
42
アナログ画像信号 S0

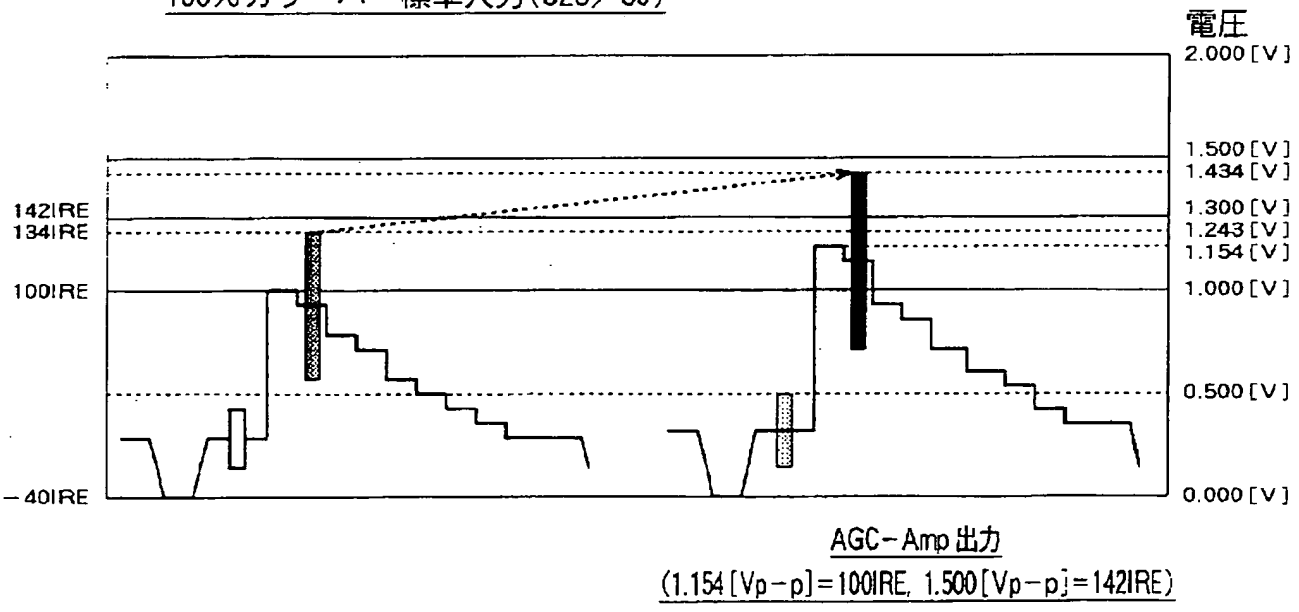
[Drawing 11]


31
アナログ画像信号 S0
プリフィルタ
11
シンクチップクランプ回路
12
A/D変換回路
13
8
リファレンス信号 S18
LPF
14
10
S14
デジタルAGC回路
30
S30
内部デジタル信号処理へ
LPF
32
S32
MAX AGC
Sync AGC
AGCゲイン検出回路
33
S33
選択信号 S39

[Drawing 5]

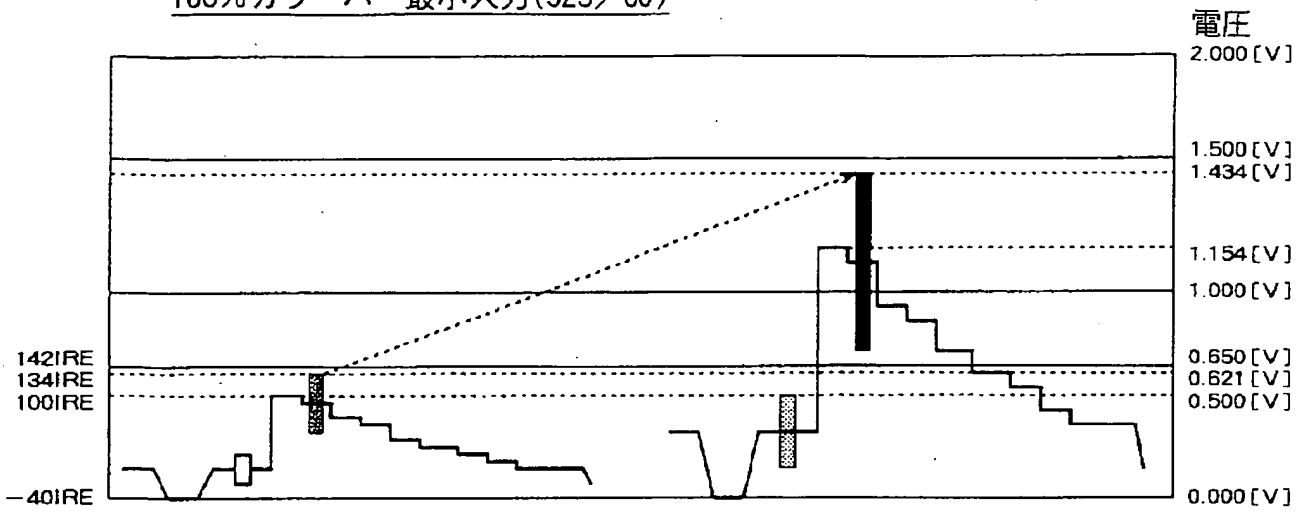


[Drawing 7]



[Drawing 8]

100%カラーバー最小入力(525／60)

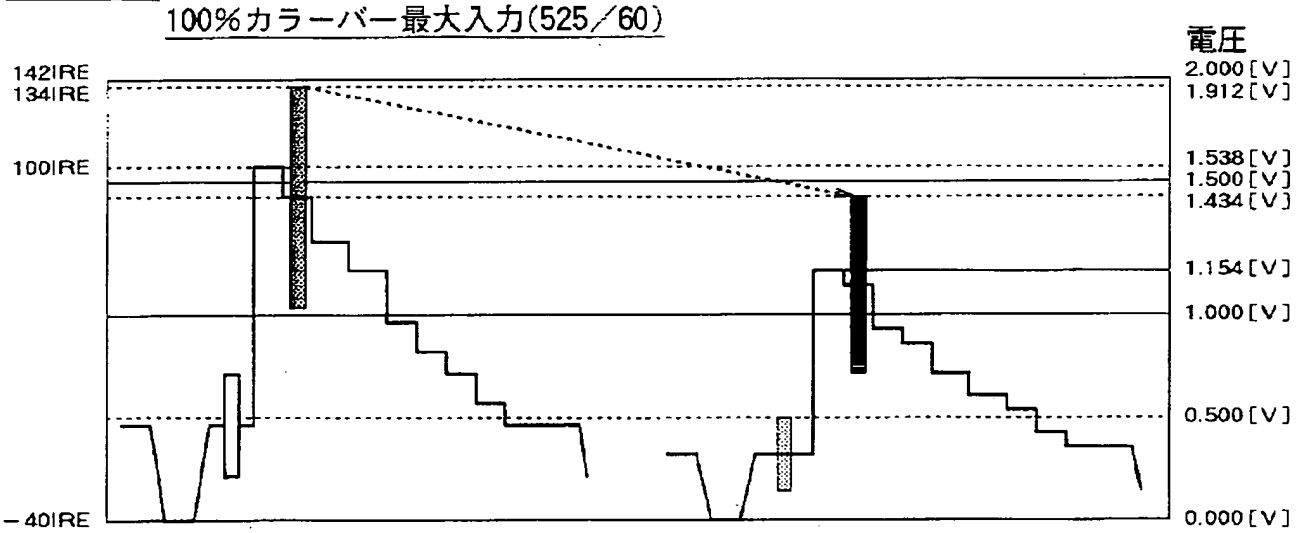


AGC−Amp出力

(1.154[Vp−p]=100IRE, 1.500[Vp−p]=142IRE)

[Drawing 9]

100%カラーバー最大入力(525／60)



AGC−Amp出力

(1.154[Vp−p]=100IRE, 1.500[Vp−p]=142IRE)

[Translation done.]

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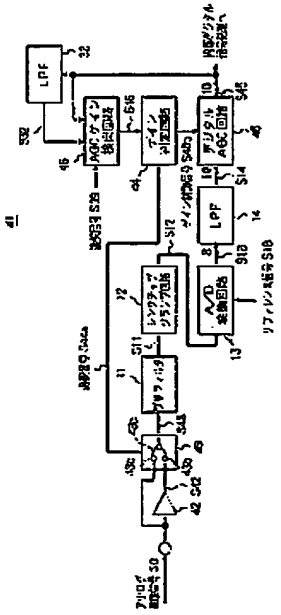
(54)【発明の名称】　画像信号処理回路

(57)【要約】

【課題】　小規模な回路構成で、ゲイン制御を高精度に行うことができ、比較的簡単に開発可能な画像信号処理回路を提供する。

【解決手段】　入力されたアナログ画像信号Ｓ０を、所定の増幅率で増幅する増幅回路４２と、選択信号Ｓ４４ａに基づいて、アナログ画像信号Ｓ０あるいはアナログ画像信号Ｓ４２を選択するセレクタ４３と、選択されたアナログ画像信号をＳ４３をＡ／Ｄ変換してデジタル画像信号Ｓ１３を生成するＡ／Ｄ変換回路１３と、制御信号Ｓ４４ｂに基づいて、デジタル画像信号Ｓ１４をゲイン制御するデジタルＡＧＣ回路４５と、ゲイン制御されたデジタル画像信号Ｓ４５のゲインを検出するＡＧＣゲイン検出回路４６と、当該ゲイン検出結果に基づいて、選択信号Ｓ４４ａおよび制御信号Ｓ４４ｂを生成するゲイン判定回路４４とを有する。



1

【特許請求の範囲】

【請求項１】入力されたアナログ画像信号を、所定のゲインで増幅する単数または複数の増幅手段と、

アナログ画像信号選択用の選択信号に基づいて、前記入力されたアナログ画像信号および前記増幅されたアナログ画像信号のうち、複数のアナログ画像信号から、一のアナログ画像信号を選択する選択手段と、

前記選択されたアナログ画像信号を、デジタル画像データに変換するアナログ／デジタル変換手段と、

制御信号に応じたゲインで、前記デジタル画像信号のレベルを調整するレベル調整手段と、

前記レベルが調整されたデジタル画像信号のゲインを検出するゲイン検出手段と、

前記検出されたゲインに基づいて、前記アナログ画像信号選択用の選択信号および前記制御信号を生成するゲイン判定手段とを有する画像信号処理回路。

【請求項２】前記ゲイン判定手段は、

前記増幅手段のゲインと、前記アナログ／デジタル変換手段の入力ダイナミックレンジと、前記ゲイン検出結果とに基づいて、

前記複数のアナログ画像信号のうち、前記アナログ／デジタル変換手段の入力ダイナミックレンジに最も近いゲインを持つアナログ画像信号を選択することを示すアナログ画像信号選択用の選択信号を生成する請求項１に記載の画像信号処理回路。

【請求項３】前記選択手段は、前記入力されたアナログ画像信号と、前記増幅されたアナログ画像信号とのうち、一のアナログ画像信号を選択する請求項１に記載の画像信号処理回路。

【請求項４】前記レベル調整手段からのデジタル画像信号から、同期信号を抽出する同期信号抽出手段をさらに有し、

前記ゲイン検出手段は、ゲイン検出信号選択用の選択信号に基づいて、前記レベル調整手段からのデジタル画像信号と、前記同期信号抽出手段からの同期信号のうち一方の信号のゲインを検出する請求項１に記載の画像信号処理回路。

【請求項５】前記同期信号抽出手段は、ローパスフィルタである請求項４に記載の画像信号処理回路。

【請求項６】前記ゲイン検出手段は、前記同期信号のゲインを検出した後に、前記デジタル画像データ信号のゲインを検出する請求項４に記載の画像信号処理回路。

【請求項７】前記ゲイン判定手段は、

アナログ画像信号選択用の選択信号によるアナログ画像信号の選択が所定の時間内に所定回数以上切り換わる場合に、アナログ画像信号選択用の選択信号を生成するときに用いる、ゲイン検出結果のゲイン判定レベルを変更する請求項１に記載の画像信号処理回路。

【請求項８】前記ゲイン判定手段は、アナログ画像信号選択用の選択信号によるアナログ画像信号の選択が所定の時間内に所定回数以上切り換わる場合に、アナログ画像信号選択用の選択信号を生成するときに用いる、ゲイン検出結果のゲイン判定レベルを下げる請求項１に記載の画像信号処理回路。

【請求項９】前記増幅手段は、固定したゲインで増幅を行う請求項１に記載の画像信号処理回路。

【請求項１０】前記増幅手段は、ゲインが可変である請求項１に記載の画像信号処理回路。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、画像信号処理回路に関する。

【０００２】

【従来の技術】例えば、受信したＮＴＳＣ(National Television Committee)方式やＰＡＬ(Phase Alternation by Line)方式のアナログ画像信号をデジタル処理する受像機のデコーダには、通常、受信したアナログ画像信号をデジタル画像データに変換するＡ(Analog)／Ｄ(Digital)変換回路が内蔵されている。また、例えば、アンテナに誘起される電波に強弱があると、受信したアナログ画像信号も同様に変動し、画面のコントラストなどが変化してしまう。これを回避するために、受像機のデコーダには、受信したアナログ画像信号のレベルを所定のレベルにするためにゲインを制御するＡＧＣ(Automatic Gain Control)回路が内蔵されている。

【０００３】以下、従来の受像機のデコーダに内蔵されたＡ／Ｄ変換回路およびＡＧＣ回路を備えた画像信号処理回路について説明する。図６は、従来の受像機のデコーダに内蔵された、アナログ方式でゲイン検出を行い、アナログ方式でゲインコントロールを行う画像信号処理回路１の構成図である。画像信号処理回路１では、輝度信号、コンポジット信号あるいは色信号などのアナログ画像信号Ｓ０を入力し、このアナログ画像信号Ｓ０をＡＧＣゲイン検出回路１６からのゲイン検出信号Ｓ１６に基づいて、ゲインコントロールアンプ１０にてゲイン制御を行う。ゲインコントロールアンプ１０からのアナログ画像信号Ｓ１０は、ローパスフィルタ（ＬＰＦ）１５、ＡＧＣゲイン検出回路１６およびプリフィルタ１１に出力される。

【０００４】アナログ画像信号Ｓ１０は、ローパスフィルタ１５にてサブキャリアなどの水平方向の高域成分が除去され、帯域が例えば１ＭＨｚに制限されたアナログ画像信号Ｓ１５がＡＧＣゲイン検出回路１６に出力される。ここで、アナログ画像信号Ｓ１５は、アナログ画像信号Ｓ０に含まれる同期信号と略同じである。ＡＧＣゲイン検出回路１６では、選択信号Ｓ１９に基づいて、ローパスフィルタ１５からのアナログ画像信号Ｓ１５およびゲインコントローアンプ１０からのアナログ画像信号Ｓ１０について選択的にゲイン検出が行われ、当該ゲイン検出に応じたゲイン制御信号Ｓ１６がゲインコントロ

ールアンプ10に出力される。

【0005】具体的には、AGCゲイン検出回路16では、アナログ画像信号S15が選択されている場合には、アナログ画像信号S0に含まれる同期信号についてゲイン検出が行われ、ゲインコントロールアンプ10において、当該同期信号について、フィードバックゲイン制御が行われる。例えば、同期信号のゲインが、NTSC方式の場合には401IREとなり、PAL方式の場合には431IREとなるように、フィードバックゲイン制御が行われる。

【0006】一方、AGCゲイン検出回路16において、アナログ画像信号S10が選択されている場合には、ゲインコントロールアンプ10およびAGCゲイン検出回路16において、アナログ画像信号S0に含まれる全帯域の信号についてゲイン制御が行われる。すなわち、アナログ画像信号S0のピークレベルが所定のレンジ内に収まるように、フィードバックゲイン制御が行われる。例えば、A/D変換回路13における入力ダイナミックレンジが1.500Vp-pであり、図7および図8に示すように、アナログ画像100%カラーバー信号S0のピークレベルが1.243Vおよび0.621Vと低い場合には、ゲインコントロールアンプ10は、ピークレベルが1.434Vとなるアナログ画像信号S10を生成するように、ゲイン制御を行う。また、図9に示すように、アナログ画像100%カラーバー信号S0のピークレベルが1.912Vと高い場合には、ゲインコントロールアンプ10は、ピークレベルが1.434Vとなるアナログ画像信号S10を生成するように、ゲイン制御を行う。

【0007】また、アナログ画像信号S10は、後段のA/D変換回路13におけるA/D変換時にエイリアシングが生じないように、プリフィルタ11において帯域制限される。この帯域制限されたアナログ画像信号S11は、シンクチップクランプ回路12において、そのボトム電位が、A/D変換回路13におけるボトム電位に調整される。アナログ画像信号S12は、A/D変換回路13において、リファレンス信号S18に応じた量子化ステップでA/D変換され、この8ビットのデジタル画像信号S13が、LPF14において、水平方向の高域成分が除去され、例えば10ビットのデジタル画像信号S14となる。

【0008】図10は、従来の受像機のデコーダに内蔵された、デジタル方式でゲイン検出を行い、アナログ方式でゲインコントロールを行う画像信号処理回路21の構成図である。画像信号処理回路21では、LPF14からのデジタル画像信号S14が、LPF22およびAGCゲイン検出回路26に出力される。デジタル画像信号S14は、LPF22において、サブキャリアなどの水平方向の高域成分が除去され、帯域が例えば1MHzに制限されてデジタル画像信号S22となる。デジタル

画像信号S22は、アナログ画像信号S0に含まれる同期信号をA/D変換したものに相当している。AGCゲイン検出回路26では、選択信号S29に基づいて、ローパスフィルタ22からのデジタル画像信号S22およびLPF14からのデジタル画像信号S14について選択的にゲイン検出が行われ、当該ゲイン検出に応じたデジタルのゲイン制御信号S26がD/A変換回路23に出力される。ゲイン制御信号S26は、D/A変換回路23にて、アナログのゲイン制御信号S23にD/A変換される。アナログ画像信号S0は、ゲイン制御信号S23に基づいて、ゲインコントロールアンプ20において、フィードバックゲイン制御される。

【0009】図11は、従来の受像機のデコーダに内蔵された、デジタル方式でゲイン検出を行い、デジタル方式でゲインコントロールを行う画像信号処理回路31の構成図である。アナログ画像信号S0が、プリフィルタ11、シンクチップクランプ回路12、A/D変換回路13およびLPF14において処理され、デジタル画像信号S14として、デジタルAGC30に入力される。デジタル画像信号S14は、デジタル形式のゲイン制御信号S33に基づいて、フィードバックゲイン制御され、デジタル画像信号S30として出力される。デジタル画像信号S30は、LPF32およびAGCゲイン検出回路33に出力される。AGCゲイン検出回路33は、同期信号に対応するデジタル画像信号S32およびデジタル画像信号S30について、選択信号S39に基づいて、選択的にゲイン検出を行い、当該検出結果に応じたゲイン制御信号S33をデジタルAGC30に出力する。

【0010】

【発明が解決しようとする課題】しかしながら、上述した図6に示す画像信号処理回路1では、AGCゲイン検出回路16からのゲイン制御信号S16によってゲインコントロールアンプ10をアナログ方式でフィードバック制御しているため、リニアなゲインコントロールを実現するのが困難であり、開発時間が長期化してしまう。具体的には、ゲインコントロールアンプ10を構成するCMOSのトランジスタが所望の特性を持つ回路を設計することが容易でない。

【0011】また、上述した図10に示す画像信号処理回路21では、AGCゲイン検出回路26においてデジタル形式でゲイン制御信号S26を生成しているため、ゲイン制御を高精度に行うことができるが、一般的にD/A変換回路23を設けていることから、回路が大規模化してしまうという問題がある。

【0012】さらに、上述した図11に示す画像信号処理回路31では、A/D変換後に、デジタル形式でゲイン制御を行うことから、アナログ画像信号S0の振幅が小さい場合には、A/D変換回路13の入力ダイナミックレンジを十分に使ったA/D変換を行うことができ

ず．量子化が荒くなり、量子化ノイズの影響で．画質劣化が著しく汚い画像となってしまう。

【００１３】本発明は、上述した従来技術に鑑みてなされ．小規模な回路構成で．ゲイン制御を高精度に行うことができ、比較的簡単に開発可能な画像信号処理回路を提供することを目的とする。

【００１４】

【課題を解決するための手段】上述した従来技術の問題点を解決し、上述した目的を達成するために、本発明の画像信号処理回路は、入力されたアナログ画像信号を、所定のゲインで増幅する単数または複数の増幅手段と、アナログ画像信号選択用の選択信号に基づいて．前記入力されたアナログ画像信号および前記増幅されたアナログ画像信号のうち、複数のアナログ画像信号から．一のアナログ画像信号を選択する選択手段と、前記選択されたアナログ画像信号を、デジタル画像データに変換するアナログ／デジタル変換手段と、制御信号に応じたゲインで．前記デジタル画像信号のレベルを調整するレベル調整手段と、前記レベル調整されたデジタル画像信号のゲインを検出するゲイン検出手段と．前記検出されたゲインに基づいて．前記アナログ画像信号選択用の選択信号および前記制御信号を生成するゲイン判定手段とを有する。

【００１５】本発明の画像信号処理回路はでは．ゲイン判定手段において、ゲイン検出結果に基づいて．選択手段において選択するアナログ画像信号を決定する。そのため．ゲイン検出結果に基づいて、例えば、入力されたアナログ画像信号の増幅率を決定することができ．アナログ／デジタル変換手段における変換時処理の入力ダイナミックレンジを効率的に使用するように、入力されたアナログ画像信号を増幅することができる。また．ゲイン判定手段において、ゲイン検出手段にて検出されたゲインに基づいて．デジタル方式のレベル調整手段を制御していることから、デジタル方式で高精度なレベル調整．すなわち．自動ゲイン制御（ＡＧＣ）を行うことができる。

【００１６】

【発明の実施の形態】以下．本発明の実施形態に係わる画像信号処理回路について説明する。従来の画像信号処理回路では、ＮＴＳＣ方式あるいはＰＡＬ方式などのアナログ画像信号をＡ／Ｄ変換するときに、アナログ方式あるいはデジタル方式のいずれか一方のみでゲイン制御を行っていたのに対して．本実施形態の画像信号処理回路では、アナログ方式およびデジタル方式の双方によって２重のフィードバック制御を行う。

【００１７】第１実施形態

図１は、本実施形態の画像信号処理回路４１の構成図である。図１に示すように．画像信号処理回路４１は、増幅回路４２、セレクタ４３．プリフィルタ１１．シンクチップクランプ回路１２．Ａ／Ｄ変換回路１３．ＬＰＦ１４．デジタルＡＧＣ回路４５、ＬＰＦ３２、ＡＧＣゲイン検出回路４６およびゲイン判定回路４４を備えている。ここで、プリフィルタ１１、シンクチップクランプ回路１２およびＡ／Ｄ変換回路１３は．図５に示す画像信号処理回路１の同一符号の構成要素と同じである。また．ＬＰＦ３２は、図１０に示す画像信号処理回路３１の同一符号の構成要素と同じである。画像信号処理回路４１は、例えば．受信したＮＴＳＣ方式やＰＡＬ方式のアナログ画像信号をデジタル処理する受像機のデコーダに内蔵されている。

【００１８】増幅回路４２は、輝度信号、コンポジット信号あるいは色信号などのアナログ画像信号Ｓ０を入力し．このアナログ画像信号Ｓ０を６ｄＢだけ増幅し、増幅されたアナログ画像信号Ｓ４２をセレクタ４３の入力端子４３ｂに出力する。セレクタ４３は、ゲイン判定回路４４からの例えば１ビットの選択信号Ｓ４４ａに基づいて．スイッチ４３ｃを入力端子Ｓ４３ａとＳ４３ｂとの間で切り換えて、アナログ画像信号Ｓ０あるいはＳ４２を選択的に．アナログ画像信号Ｓ４３としてプリフィルタ１１に出力する。

【００１９】プリフィルタ１１は、Ａ／Ｄ変換時にエイリアシングが発生しないように、アナログ画像信号Ｓ４３に対してフィルタ処理を行い、周波数を所定の帯域に制限する。シンクチップクランプ回路１２は、プリフィルタ１１からのアナログ画像信号Ｓ１１のボトム電位を．Ａ／Ｄ変換回路１３におけるＡ／Ｄ変換でのボトム電位に調整し．この調整されたアナログ画像信号Ｓ１２をＡ／Ｄ変換回路１３に出力する。

【００２０】Ａ／Ｄ変換回路１３は．アナログ画像信号Ｓ１２を、リファレンス信号Ｓ１８に応じた量子化ステップでＡ／Ｄ変換し、８ビットのデジタル画像信号Ｓ１３をＬＰＦ１４に出力する。ＬＰＦ１４は、デジタル画像信号Ｓ１３に対して、フィルタ処理を行い、水平方向の広域成分を除去し、例えば１０ビットのデジタル画像信号Ｓ１４をデジタルＡＧＣ回路４５に出力する。

【００２１】デジタルＡＧＣ回路４５は、ゲイン判定回路４４からのゲイン制御信号Ｓ４４ｂに基づいて．デジタル画像信号Ｓ１４に対してデジタル方式のフィードバックゲイン制御を行い、当該ゲイン制御されたデジタル画像信号Ｓ４５を出力する。ＬＰＦ３２は、デジタルＡＧＣ回路４５からのデジタル画像信号Ｓ４５に対して、サブキャリアなどの水平方向の高域成分を除去し．帯域が例えば約１ＭＨｚに制限されたデジタル画像信号Ｓ３２をＡＧＣゲイン検出回路４６に出力する。デジタル画像信号Ｓ３２は．アナログ画像信号Ｓ０に含まれる同期信号に対応したデジタル信号である。

【００２２】ＡＧＣゲイン検出回路４６は、選択信号Ｓ３９に応じて．ＬＰＦ３２からのデジタル画像信号Ｓ３２とデジタルＡＧＣ回路４５からのデジタル画像信号Ｓ４５とについて．選択的に．デジタル方式でゲイン検出

を行い、当該検出結果に応じたゲイン検出信号Ｓ４６をゲイン判定回路４４に出力する。具体的には、選択信号Ｓ３９がシンクレベルの検出を指示している場合には、ＡＧＣゲイン検出回路４６は、デジタル画像信号Ｓ３２のゲイン検出を行い、デジタル画像信号Ｓ４５に含まれる同期信号のシンクレベルを検出する。一方、選択信号Ｓ３９がマックスレベルの検出を指示している場合には、ＡＧＣゲイン検出回路４６は、デジタル画像信号Ｓ４５のゲイン検出を行い、デジタル画像信号Ｓ４５のピークレベルを検出する。例えば、選択信号Ｓ３９がシンクレベルの検出を指示した後にマックスレベルの検出を指示するようにすることで、デジタルＡＧＣ回路４５においてデジタル画像信号Ｓ４５のシンクレベルを調整した後にピークレベルを調整することができる。

【００２３】ゲイン判定回路４４は、ゲイン検出信号Ｓ４６に基づいて、アナログ画像信号Ｓ１２の振幅に対して、Ａ／Ｄ変換回路１３の入力ダイナミックレンジが余裕があるか否かを判断し、余裕があると判断した場合には、入力端子４３ｂに切り換えることを示す選択信号Ｓ４４ａをセレクタ４３に出力する。ここで、Ａ／Ｄ変換回路１３の入力ダイナミックレンジは、例えば、０～１．５００Ｖである。一方、ゲイン判定回路４４は、アナログ画像信号Ｓ１２の振幅に対して、Ａ／Ｄ変換回路１３の入力ダイナミックレンジが余裕がないと判断しが場合には、入力端子４３ａに切り換えることを示す選択信号Ｓ４４ａをセレクタ４３に出力する。具体的には、ゲイン検出信号Ｓ４６に基づいて、アナログ画像信号Ｓ１２のピークレベルが、Ａ／Ｄ変換回路１３の入力ダイナミックレンジの半分以下である場合には余裕があると判断し、半分より大きい場合には余裕がないと判断する。

【００２４】また、ゲイン判定回路４４は、ゲイン検出信号Ｓ４６に基づいて、デジタル画像信号Ｓ４５をデジタルＡＧＣ回路４５において所定のレベルにフィードバックゲイン制御するためのゲイン制御信号Ｓ４４ｂを生成し、これをデジタルＡＧＣ回路４５に出力する。

【００２５】以下、図１に示す画像信号処理回路４１の動作について説明する。先ず、アナログ画像信号Ｓ０の振幅のピークが、Ａ／Ｄ変換回路１３の入力ダイナミックレンジ（１．５００Ｖ）の半分（０．７５０Ｖ）以下である場合について説明する。この場合には、ゲイン検出信号Ｓ４６に基づいて、ゲイン判定回路４４において、スイッチを入力端子４３ｂに切り換えることを示す選択信号Ｓ４４ａがセレクタ４３に出力され、アナログ画像信号Ｓ０を６ｄＢだけ増幅したアナログ画像信号Ｓ４２がアナログ画像信号Ｓ４３としてプリフィルタ１１に出力される。すなわち、アナログ画像信号Ｓ０の振幅を２倍にしたアナログ画像信号Ｓ４３がプリフィルタ１１に出力される。

【００２６】アナログ画像信号Ｓ４３は、プリフィルタ１１において帯域制限され、シンクチップクランプ回路１２においてボトム電位が調整され、Ａ／Ｄ変換回路１３においてＡ／Ｄ変換され、８ビットのデジタル画像信号Ｓ１３としてＬＰＦ１４に出力される。デジタル画像信号Ｓ１３は、ＬＰＦ１４において、水平方向の高域成分が除去され、１０ビットのデジタル画像信号Ｓ１４となる。デジタル画像信号Ｓ１４は、アナログ画像信号Ｓ３２を選択することを示す選択信号Ｓ３９に基づいて、先ず、デジタルＡＧＣ回路４５、ＬＰＦ３２、ＡＧＣゲイン検出回路４６およびゲイン判定回路４４によるデジタル方式のフィードバック制御によって、シンクレベルが、例えば、ＮＴＳＣ方式の場合には４０１ｉＲＥになるように、ＰＡＬ方式の場合には４３１ｉＲＥになるように、ゲイン制御される。次に、アナログ画像信号Ｓ４５を選択することを示すように選択信号Ｓ３９が切り換わり、デジタル画像信号Ｓ１４は、デジタルＡＧＣ回路４５、ＡＧＣゲイン検出回路４６およびゲイン判定回路４４によるデジタル方式のフィードバック制御によって、ピークレベルが規定のレンジいっぱいになるようにゲイン制御される。

【００２７】次に、アナログ画像信号Ｓ０の振幅のピークが、Ａ／Ｄ変換回路１３の入力ダイナミックレンジ（１．５００Ｖ）の半分（０．７５０Ｖ）より大きい場合について説明する。この場合には、ゲイン検出信号Ｓ４６に基づいて、ゲイン判定回路４４において、スイッチを入力端子４３ａに切り換えることを示す選択信号Ｓ４４ａがセレクタ４３に出力され、アナログ画像信号Ｓ０がアナログ画像信号Ｓ４３としてプリフィルタ１１に出力される。

【００２８】アナログ画像信号Ｓ４３は、プリフィルタ１１において帯域制限され、シンクチップクランプ回路１２においてボトム電位が調整され、Ａ／Ｄ変換回路１３においてＡ／Ｄ変換され、８ビットのデジタル画像信号Ｓ１３としてＬＰＦ１４に出力される。デジタル画像信号Ｓ１３は、ＬＰＦ１４において、水平方向の高域成分が除去され、１０ビットのデジタル画像信号Ｓ１４となる。その後の処理は、前述したアナログ画像信号Ｓ０の振幅のピークが入力ダイナミックレンジ（１．５００Ｖ）の半分（０．７５０Ｖ）以下である場合と同じである。

【００２９】以上説明したように、画像信号処理回路４１では、デジタルＡＧＣ回路４５、ＡＧＣゲイン検出回路４６およびゲイン判定回路４４によって、デジタル方式で、デジタル画像信号Ｓ１４のゲインをフィードバック制御するため、高精度なゲイン制御を行うことができる。すなわち、画像信号処理回路４１によれば、ＮＴＳＣ方式あるいはＰＡＬ方式のアナログ画像信号Ｓ０をＡ／Ｄ変換して得られた高品質のデジタル画像信号を、後段のデジタル信号処理回路に出力することができる。また、画像信号処理回路４１では、アナログ画像信号Ｓ０

のピークレベルの振幅が、A／D変換回路13の入力ダイナミックレンジの半分以下と非常に低い場合には、アナログ画像信号S0の振幅を2倍に増幅したアナログ画像信号S12をA／D変換回路13に出力する。そのため、振幅のピークレベルが低いアナログ画像信号S0に対して、前述した図10に示す画像信号処理回路31のように量子化精度が荒くなってしまうことを効果的に回避でき、量子化ノイズの影響を低減できる。

【0030】また、画像信号処理回路41によれば、セレクタ43に数ビットの選択信号S44aを出力するのみで、図5に示す画像信号処理回路1のように所望の特性を持たせることが困難なアナログ方式のゲインコントロールを行わないため、回路設計が容易であり、開発期間も短い。

【0031】さらに、画像信号処理回路41では、図9に示す画像信号処理回路21のように、D／A変換回路を用いないため、小規模な回路構成を実現できる。

【0032】すなわち、画像信号処理回路41によれば、アナログ画像信号S0に対して、ゲイン判定回路44、増幅回路42およびセレクタ43によってアナログ方式で荒いゲイン制御を行い、A／D変換後に、デジタルAGC回路45、AGCゲイン検出回路46およびゲイン判定回路44によってデジタル方式でゲイン制御を細かく行うことで、量子化ノイズの影響が少ない高精度なゲイン制御が行え、回路設計が容易で開発期間が短く、しかも、回路を比較的小規模にできる。

【0033】第2実施形態

図2は、本実施形態の画像信号処理回路51の構成図である。図2に示すように、画像信号処理回路51は、増幅回路56，57，58，59、セレクタ53、プリフィルタ11、シンクチップクランプ回路12、A／D変換回路13、コラムデコーダ14、デジタルAGC回路45、LPF32、AGCゲイン検出回路46およびゲイン判定回路54を有する。ここで、図2に示すプリフィルタ11、シンクチップクランプ回路12、A／D変換回路13、コラムデコーダ14、デジタルAGC回路45、LPF32およびAGCゲイン検出回路46は、図1に示す同一符号の構成要素と同じである。

【0034】増幅回路56は、アナログ画像信号S0を入力し、このアナログ画像信号S0を－3dBだけ増幅し、増幅されたアナログ画像信号S56をセレクタ53に出力する。増幅回路57は、アナログ画像信号S0を入力し、このアナログ画像信号S0を3dBだけ増幅し、増幅されたアナログ画像信号S57をセレクタ53に出力する。増幅回路58は、アナログ画像信号S0を入力し、このアナログ画像信号S0を6dBだけ増幅し、増幅されたアナログ画像信号S58をセレクタ53に出力する。増幅回路59は、アナログ画像信号S0を入力し、このアナログ画像信号S0を9dBだけ増幅し、増幅されたアナログ画像信号S59をセレクタ53に出力する。

【0035】ゲイン判定回路54は、ゲイン検出信号S46に基づいて、2ビットの選択信号S54aをセレクタ53に出力する。具体的には、ゲイン判定回路54は、ゲイン検出信号S46に基づいて、アナログ画像信号S12のピークレベルが、A／D変換回路13の入力ダイナミックレンジを越えている場合もしくはA／D変換後最大値に張り付いている場合には、アナログ画像信号S56を選択することを示す選択信号S54aを出力する。また、ゲイン判定回路54は、ゲイン検出信号S46に基づいて、アナログ画像信号S12のピークレベルが、A／D変換回路13の入力ダイナミックレンジの1倍以下で$1/2^{1/4}$倍より大きい場合には、アナログ画像信号S0を選択することを示す選択信号S54aを出力する。

【0036】また、ゲイン判定回路54は、ゲイン検出信号S46に基づいて、アナログ画像信号S12のピークレベルが、A／D変換回路13の入力ダイナミックレンジの$1/2^{1/4}$倍以下で1／2倍より大きい場合には、アナログ画像信号S57を選択することを示す選択信号S54aを出力する。また、ゲイン判定回路54は、ゲイン検出信号S46に基づいて、アナログ画像信号S12のピークレベルが、A／D変換回路13の入力ダイナミックレンジの1／2倍以下で$1/(2\times 2^{1/4})$倍より大きい場合には、アナログ画像信号S58を選択することを示す選択信号S54aを出力する。さらに、ゲイン判定回路54は、ゲイン検出信号S46に基づいて、アナログ画像信号S12のピークレベルが、A／D変換回路13の入力ダイナミックレンジの$1/(2\times 2^{1/4})$倍以下ではアナログ画像信号S59を選択することを示す選択信号S54aを出力する。

【0037】図2に示す画像信号処理回路51の動作について簡単に説明する。画像信号処理回路51の動作は、ゲイン判定回路54からの選択信号S54aに基づいて、セレクタ53においてアナログ画像信号S0，S56、S57、S58，S59のうち何れか一つを選択する点を除いて、図1に示す画像信号処理回路41と同じである。

【0038】すなわち、ゲイン検出信号S46に基づいて、ゲイン判定回路54において、アナログ画像信号S0、S56，S57，S58，S59のうち何れを選択するかを示す選択信号S54aがセレクタ53に出力され、当該選択信号S54aに基づいて、増幅されたアナログ画像信号S56，S57，S58、S59あるいはアナログ画像信号S0が、セレクタ53によって選択され、アナログ画像信号S53としてプリフィルタ11に出力される。

【0039】アナログ画像信号S53は、プリフィルタ11において帯域制限され、シンクチップクランプ回路12においてボトム電位が調整され、A／D変換回路1

3においてA／D変換され．8ビットのデジタル画像信号S13としてLPF14に出力される。デジタル画像信号S13は．LPF14において．水平方向の高域成分が除去され．10ビットのデジタル画像信号S14となる。

【0040】デジタル画像信号S14は、アナログ画像信号S32を選択することを示す選択信号S39に基づいて．先ず、デジタルAGC回路45．LPF32、AGCゲイン検出回路46およびゲイン判定回路44によるデジタル方式のフィードバック制御によって．シンクレベルが、例えば、NTSC方式の場合には401IREになるように．PAL方式の場合には431IREになるように、ゲイン制御される。次に．アナログ画像信号S45を選択することを示すように選択信号S39が切り換わり、デジタル画像信号S14は、デジタルAGC回路45、AGCゲイン検出回路46およびゲイン判定回路44によるデジタル方式のフィードバック制御によって、ピークレベルが規定のレンジいっぱいになるようにゲイン制御される。

【0041】以上説明したように、画像信号処理回路51によれば、ゲイン判定回路54、増幅回路56、57，58，59およびセレクタ53によって、アナログ方式によるフィードバック制御を、図1に示す画像信号処理回路41に比べて細かく行うため．画像信号処理回路41に比べて．さらに高精度のゲイン制御を行うことができる。

【0042】第3実施形態

図3は、本実施形態の画像信号処理回路61の構成図である。図3に示すように．画像信号処理回路61は、基本的には、図1に示す画像信号処理回路41と同じであるが．ゲイン判定回路64の構成がゲイン判定回路44とは異なる。すなわち、ゲイン判定回路64は．図4に示されるゲイン判定レベルシフト回路70を備えており．ゲイン判定回路44の機能に加えて、選択信号S44aを切り換える基準となるゲイン判定レベル（0．750Vp－p）付近で、ゲイン検出信号S46によって示されるシンクレベルあるいはピークレベルが変動している場合に、セレクタ43のスイッチが頻繁に切り換わることを回避する機能を備えている。

【0043】以下、ゲイン判定レベルシフト回路70について説明する。図4に示すように．ゲイン判定レベルシフト回路70は、比較回路71、フィールドカウンタ72．AND回路73およびレベルシフト判定回路74を有する。比較回路71は．AGCゲイン検出回路46からのゲイン検出信号S46と、選択信号S44aを生成するときのゲイン判定レベルとの比較を行い．例えば．ゲイン検出信号S46が示すレベルがゲイン判定レベルに比べて大きい場合に．ハイレベルとなる比較信号S71をAND回路73に出力する。

【0044】フィールドカウンタ72は、デジタル画像信号S32あるいはS45を入力し．これらに含まれる垂直同期信号に基づいて．フィールド毎に、所定時間だけハイレベルになるフィールド検出パルス信号S72をAND回路73およびレベルシフト判定回路74に出力する。

【0045】AND回路73は、フィールド検出パルス信号S72がハイレベルのときの比較信号S71のレベルを．演算信号S73としてレベルシフト判定回路74に出力する。

【0046】レベルシフト判定回路74は、フィールド検出パルス信号S72に基づいてフィールド数をカウントすると共に．演算信号S73に含まれるパルス数をカウントする。また、レベルシフト判定回路74は．所定数のフィールド内に、演算信号S73に何個のパルスが発生するかを検出することで、選択信号S44bの切り換わりの頻度を得る。そして、レベルシフト判定回路74は．所定数のフィールド内に、所定の回数以上．選択信号S44bが切り換わったと判断すると、ゲイン判定レベルを例えば0．750から0．500Vに下げる。

【0047】以上説明したように、画像信号処理回路61によれば、ゲイン判定レベルシフト回路70を用いることで、ゲイン検出信号S46が示すレベルが．ゲイン判定レベル付近で変動した場合でも．セレクタ43が頻繁に切り換わることを効果的に回避し．高画質の画像を安定して提供することを可能にする。

【0048】本発明は上述した実施形態には限定されない。例えば、図1～3に示す増幅回路の数およびゲインは．上述した実施形態に示すものには限定されず．A／D変換回路13の入力ダイナミックレンジおよび要求される精度に応じて任意に変更可能である。また．図4に示すゲイン判定レベルシフト回路70の回路構成も、種々に変更可能である。例えば、フィールドカウンタ72を設けるのではなく、所定の時間を計測するタイマなどを用いてもよい。

【0049】また、上述した実施形態では、図1～3に示す増幅回路42，56．57，58．59として、ゲインが固定のものを例示したが、図5（A），（B），（C）に示すようなゲインが可変の増幅回路を用いてもよい。この場合には、アナログ画像信号S0およびA／D変換回路13の入力ダイナミックレンジに応じて、増幅回路のゲインを例えばユーザが調整する。図5（A）に示す増幅回路は、入力端子90と出力端子91との間に．5個の抵抗R1が直列に接続され．抵抗相互間から端子92a，92b，92c，92dが引き出されている。また、端子92a，92b，92c，92dと、オペアンプ93の－入力端子とを選択的に接続するスイッチ94が設けられている。オペアンプ93の出力端子は．出力端子91に接続されている。図5（A）に示す増幅回路では．ゲインに応じて、スイッチ94を端子92a．92b．92c，92dに選択的に接続する。こ

のとき、スイッチ94が端子92aから92dに向かって切り換わるにつれて、ゲインは低くなる。

【0050】また、図5（B）に示す増幅回路は、スイッチ104が端子102a，102b，102c，102dに選択的に接続され．これによって、抵抗R3，R4，R5，R6の何れかを介して、オペアンプ103の一入力端子と出力端子101とが接続される。

【0051】さらに、図5（C）に示す増幅回路は、スイッチ114が端子112a，112b，112c，112dに選択的に接続され．これによって、抵抗R7，R8，R9，R10の何れかを介して．オペアンプ113の一入力端子と入力端子110とが接続される。

【0052】

【発明の効果】以上説明したように．本発明の画像信号処理回路によれば、小規模な回路構成で、ゲイン制御を高精度に行うことができ．しかも比較的簡単に開発できる。

【図面の簡単な説明】

【図1】図1は．本発明の第1実施形態に係わる画像信号処理回路の構成図である。

【図2】図2は．本発明の第2実施形態に係わる画像信号処理回路の構成図である。

【図3】図3は．本発明の第3実施形態に係わる画像信号処理回路の構成図である。

【図4】図4は．図3に示すゲイン判定回路に備えられたゲイン判定レベルシフト回路の構成図である。

＊【図5】図5は．図1～3に示す増幅回路として用いることができるゲイン可変の増幅回路である。

【図6】図6は．従来の受像機のデコーダに内蔵された．アナログ方式でゲイン検出を行い．アナログ方式でゲインコントロールを行う画像信号処理回路の構成図である。

【図7】図7は．図6に示す画像信号処理回路におけるゲイン制御を説明するための図である。

【図8】図8は．図6に示す画像信号処理回路におけるゲイン制御を説明するための図である。

【図9】図9は．図6に示す画像信号処理回路におけるゲイン制御を説明するための図である。

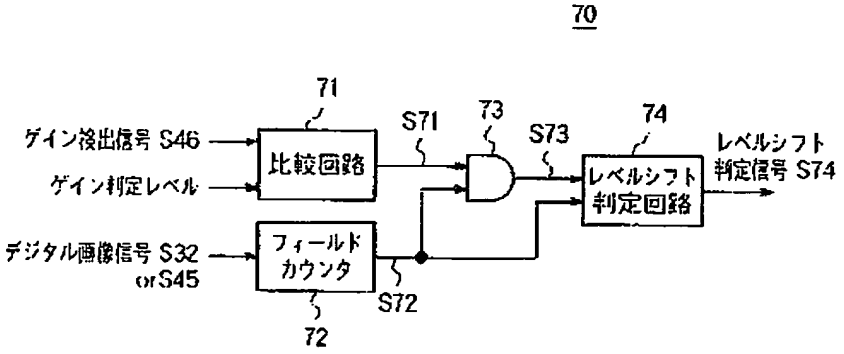
【図10】図10は、従来の受像機のデコーダに内蔵された．デジタル方式でゲイン検出を行い、アナログ方式でゲインコントロールを行う画像信号処理回路の構成図である。

【図11】図11は、従来の受像機のデコーダに内蔵された．デジタル方式でゲイン検出を行い、デジタル方式でゲインコントロールを行う画像信号処理回路の構成図である。

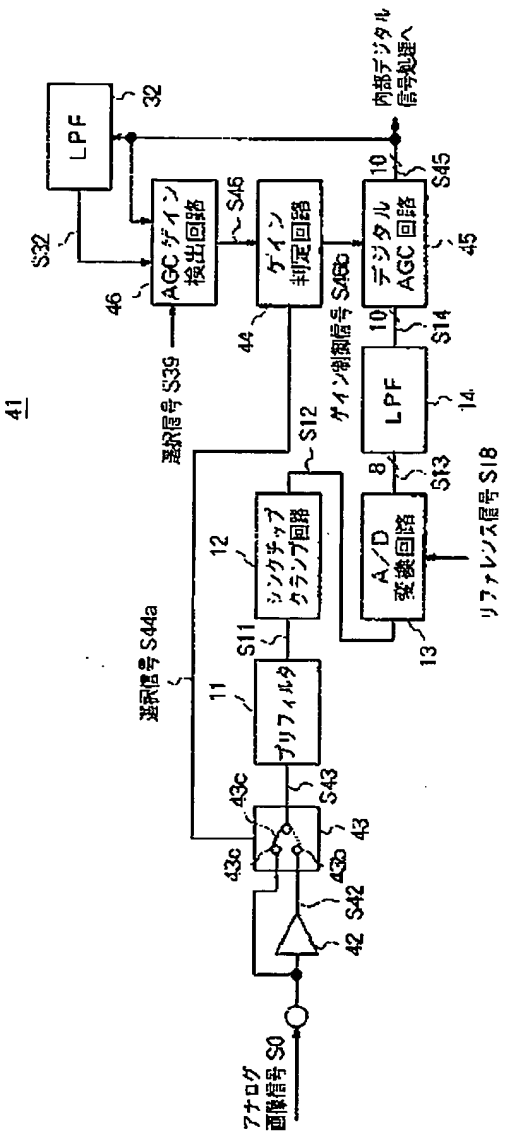
【符号の説明】

11…プリフィルタ、12…シンクチップクランプ回路．13…A／D変換回路．14，32…LPF．44，54，64…ゲイン判定回路、46…AGCゲイン検出回路、42，56，57，58，59…増幅回路、43，53…セレクタ

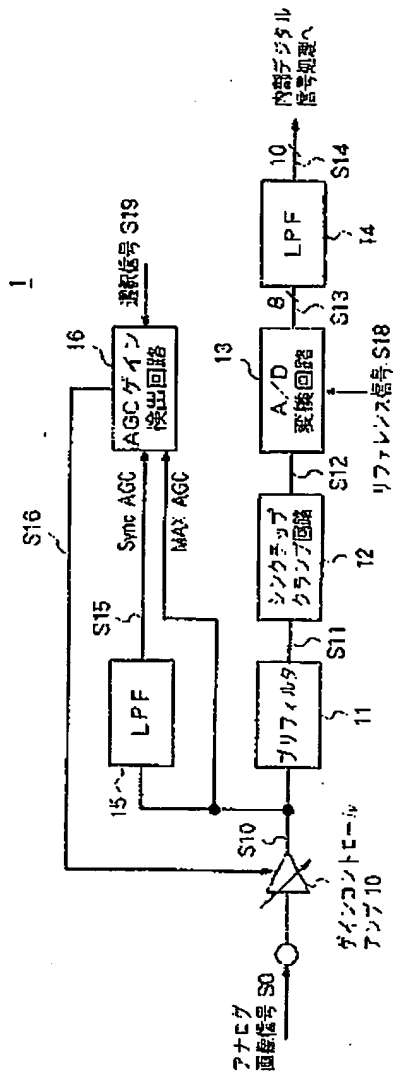
【図4】



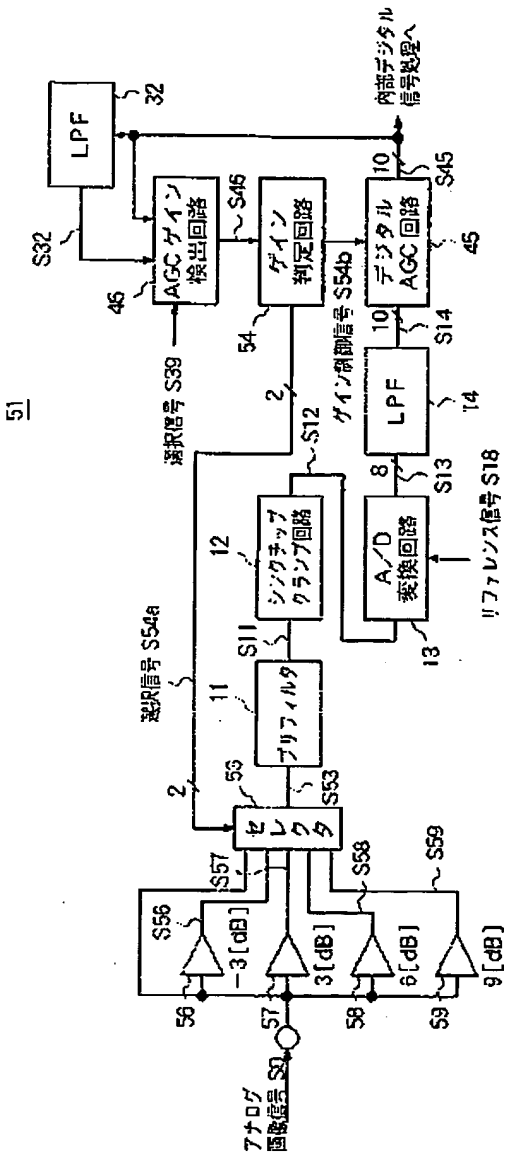
【図1】


41
LPF
32
S32
AGCゲイン検出回路
S46
ゲイン判定回路
S46a
デジタルAGC回路
45
内部デジタル信号処理へ
S45
10
46
選択信号 S39
44
ゲイン制御信号 S46a
S14
LPF
14
S12
S13
8
A/D変換回路
13
リファレンス信号 S18
シンクチップクランプ回路
12
S11
プリフィルタ
11
選択信号 S44a
43c
43b
43
S43
S42
42
アナログ画像信号 S0

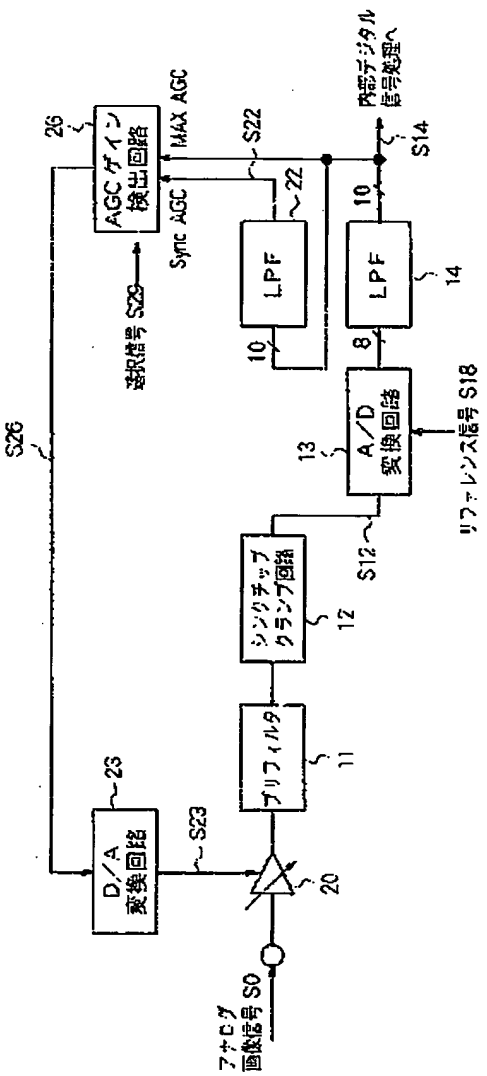
【図6】


1
内部デジタル信号処理へ
10
S14
LPF
14
8
S13
A/D変換回路
13
リファレンス信号 S18
S12
シンクチップクランプ回路
12
S11
プリフィルタ
11
ゲインコントロールアンプ 10
S10
アナログ画像信号 S0
選択信号 S19
16
AGCゲイン検出回路
Sync AGC
MAX AGC
S15
LPF
15
S16

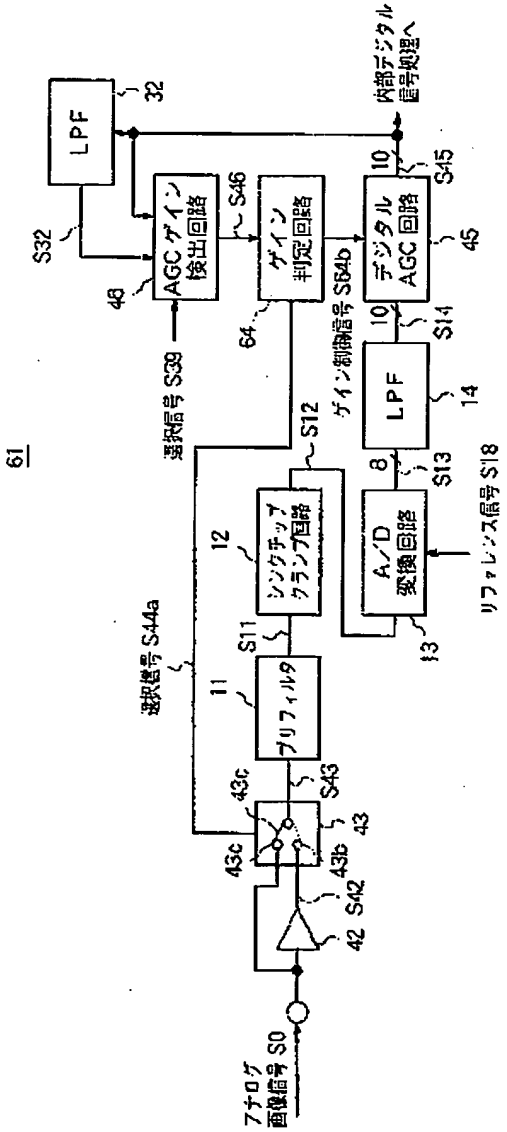
【図2】


51
LPF
32
S32
AGC ゲイン 検出回路
S46
ゲイン 判定回路
S54b
デジタル AGC 回路
S45
内部デジタル 信号処理へ
46
45
54
10
S14
選択信号 S39
ゲイン制御信号
2
S12
LPF
14
S13
8
12
シンクチップ クランプ回路
A/D 変換回路
S11
13
リファレンス信号 S18
選択信号 S54a
11
プリフィルタ
55
S53
セレクタ
S57
S58
S59
S56
-3[dB]
3[dB]
6[dB]
9[dB]
56
57
58
59
アナログ 画像信号 S0

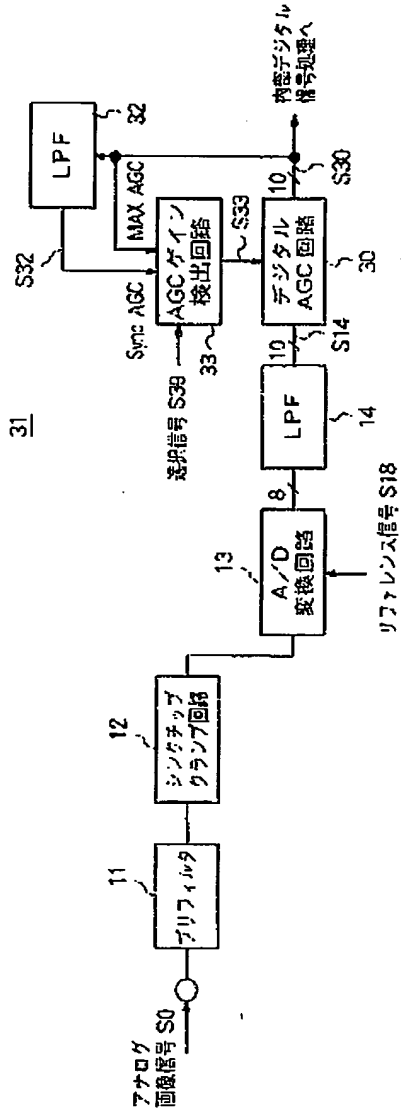
【図10】


21
26
AGC ゲイン 検出回路
MAX AGC
Sync AGC
S22
内部デジタル 信号処理へ
S14
選択信号 S29
LPF
22
10
LPF
14
8
A/D 変換回路
13
リファレンス信号 S18
S26
S12
シンクチップ クランプ回路
12
プリフィルタ
11
23
D/A 変換回路
S23
20
アナログ 画像信号 S0

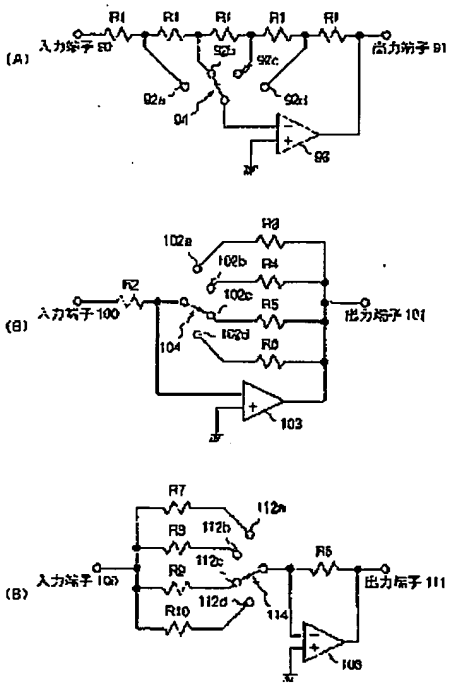
【図3】


61
LPF
32
S32
AGCゲイン検出回路
48
S46
ゲイン判定回路
64
デジタルAGC回路
10
45
S45
内部デジタル信号処理へ
選択信号 S39
ゲイン制御信号 S64b
S12
LPF
10
14
S14
S13
8
A/D変換回路
13
リファレンス信号 S18
シングチップクランプ回路
12
S11
プリフィルタ
11
選択信号 S44a
43c
S43
43
43b
S42
42
アナログ画像信号 S0

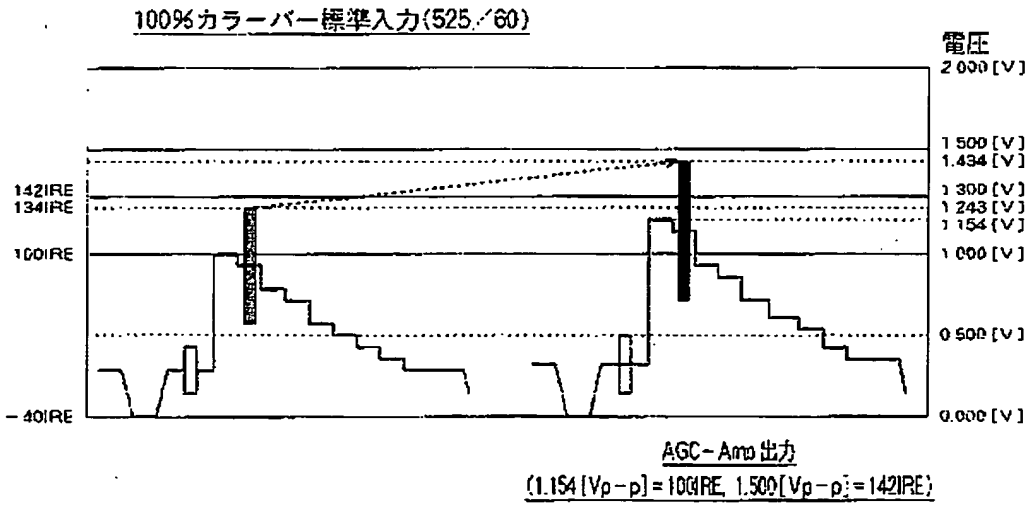
【図11】


31
LPF
32
S32
MAX AGC
Sync AGC
AGCゲイン検出回路
S33
33
デジタルAGC回路
10
30
S30
内部デジタル信号処理へ
選択信号 S38
LPF
10
14
S14
8
A/D変換回路
13
リファレンス信号 S18
シングチップクランプ回路
12
プリフィルタ
11
アナログ画像信号 S0

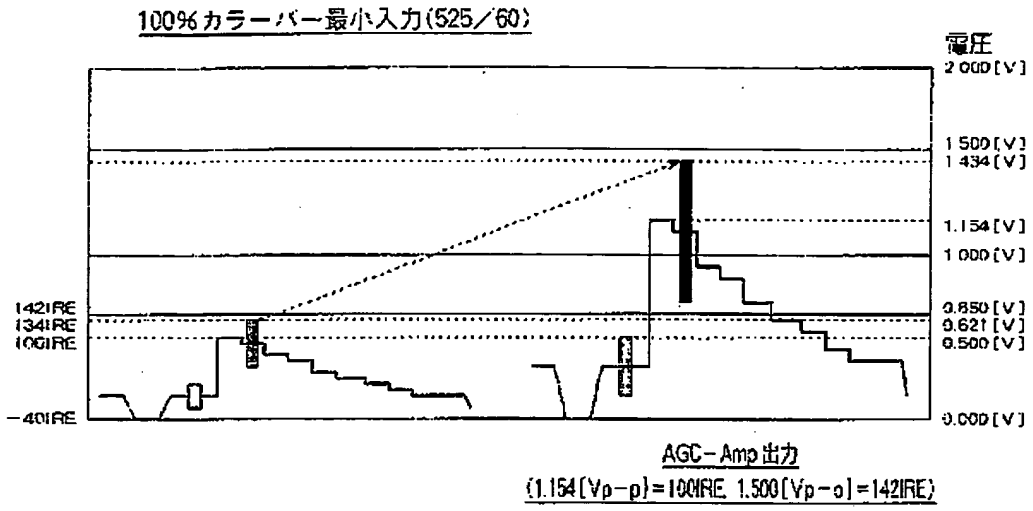
【図5】


(A)
入力端子 90
出力端子 91
92a
92b
92c
92d
94
96
(B)
入力端子 100
出力端子 101
102a
102b
102c
102d
104
103
(B)
入力端子 109
出力端子 111
112a
112b
112c
112d
114
108

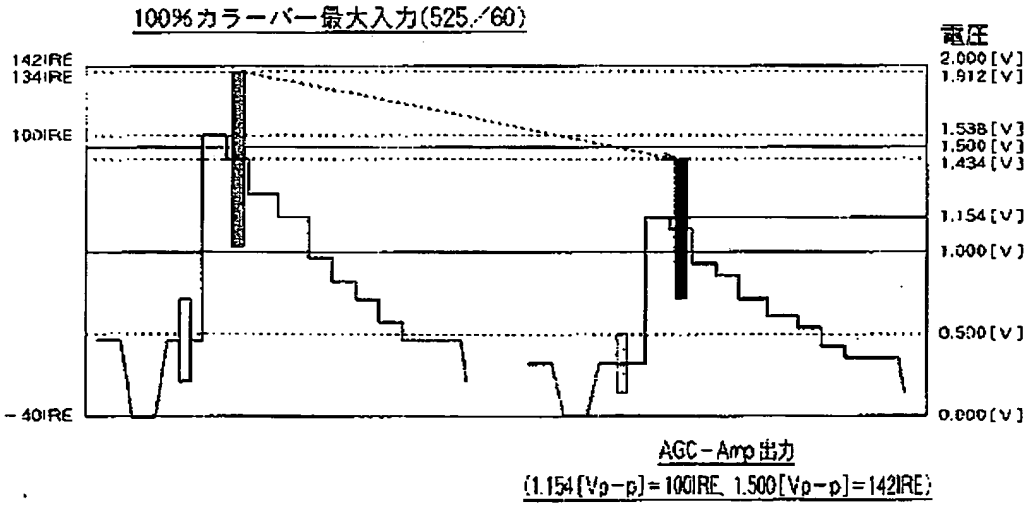
【図7】


100%カラーバー標準入力(525/60)
電圧
2.000 [V]
1.500 [V]
1.434 [V]
1.300 [V]
1.243 [V]
1.154 [V]
1.000 [V]
0.500 [V]
0.000 [V]
142IRE
134IRE
100IRE
-40IRE
AGC-Amp出力
(1.154 [Vp-p] = 100IRE, 1.500 [Vp-p] = 142IRE)

【図8】


100%カラーバー最小入力(525/60)
電圧
2.000[V]
1.500[V]
1.434[V]
1.154[V]
1.000[V]
0.850[V]
0.621[V]
0.500[V]
0.000[V]
142IRE
134IRE
100IRE
-40IRE
AGC-Amp出力
(1.154[Vp-p]=100IRE, 1.500[Vp-p]=142IRE)

【図9】


100%カラーバー最大入力(525/60)
電圧
142IRE
134IRE
100IRE
-40IRE
2.000[V]
1.912[V]
1.538[V]
1.500[V]
1.434[V]
1.154[V]
1.000[V]
0.500[V]
0.000[V]
AGC-Amp出力
(1.154[Vp-p]=100IRE, 1.500[Vp-p]=142IRE)